SNO-STR-97-035

The SNO Trigger System

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October 12, 1997

1 Introduction

The purpose of this document is to provide a complete description of the SNO trigger system. It is not, however, a "User's Guide" to the operation of the system nor is it a description of the trigger sytem's performance. A memo describing the full perfomance will not be possible until the system is installed and running underground.

The document is divided into three basic parts, each with a higher level of detail than the preceding pieces. The first part (Section 2), is a general overview intended for anyone interested in the basic conceptual design and core features of the trigger. The second part, Sections 3- 9, is a set of detailed board-by-board descriptions addressed to those interested in the full complement and implementation of trigger features. Details about the analog design, the initialization and set-up of the digital end, and a few preliminary performance measurements can be found in these sections. The last part is a set of appendices which comprise a reference for those needing to know the bit-by-bit details (memory bit map, register list, etc.).

Because of the hierarchical nature of this organization, we have attempted to make each section self-contained; the document need not be read front to back. For that reason, some information may be repeated in several sections—which accounts somewhat for the document's length.

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2 Overview

The SNO trigger system is primarily responsible for determining which events in the detector are worth saving and writing to tape for analysis. The basic idea of the trigger is conceptually very simple: if a pre-determined number of PMT's fire in coincidence, the front end electronics are signalled to save any data they may have. The data are later collected by the data acquisition system and built into events which are written to tape.

In addition to this fundamental feature, the trigger handles nearly all system-wide hardware functions. For example, calibration of the electronics (slopes and pedestals) requires a DAQ-controllable source of pulses of variable delays and widths, and the trigger system provides both the pulses and the interface to the front end electronics for these calibrations. In addition, the trigger is reponsible for ensuring synchronization of all the global trigger ('event number') counters for all the channels in the system, for keeping a master clock for measurement of time between events, and for interfacing to the GPS system for keeping absolute time for astronomical measurements.

Figure 1 depicts the entire trigger system. As the Figure indicates, the system as a whole divides into two distinct halves: an analog front end which takes DC-coupled signals initiated by the PMT pulses and sums them up, and a digital back end which determines whether an event has occured and handles the writing of trigger-related data (clocks, trigger IDs, etc.) to memory and ultimately the SNO data stream. Also shown in the Figure is the fact that the trigger system involves nearly every board in the SNO electronics:

- *FEC32 Daughterboards (DB)*: As the front end of the entire system, the DB's are responsible for the initial sum of trigger pulses initiated by PMT firings. There are eight channels summed on each DB, and there are approximately 1200 DB's in the entire system.

- *FEC32 Motherboards (MB)*: The motherboards are responsible for summing the analog sums from pairs of DB's (the two DB's on the top of the MB's are summed together and the two DB's on the bottom are summed together, resulting in two separate signals leaving each FEC). There are approximately 300 MB's in the full system.

- *SNO Backplane (BP)*: The backplanes carry the analog trigger signals from each MB

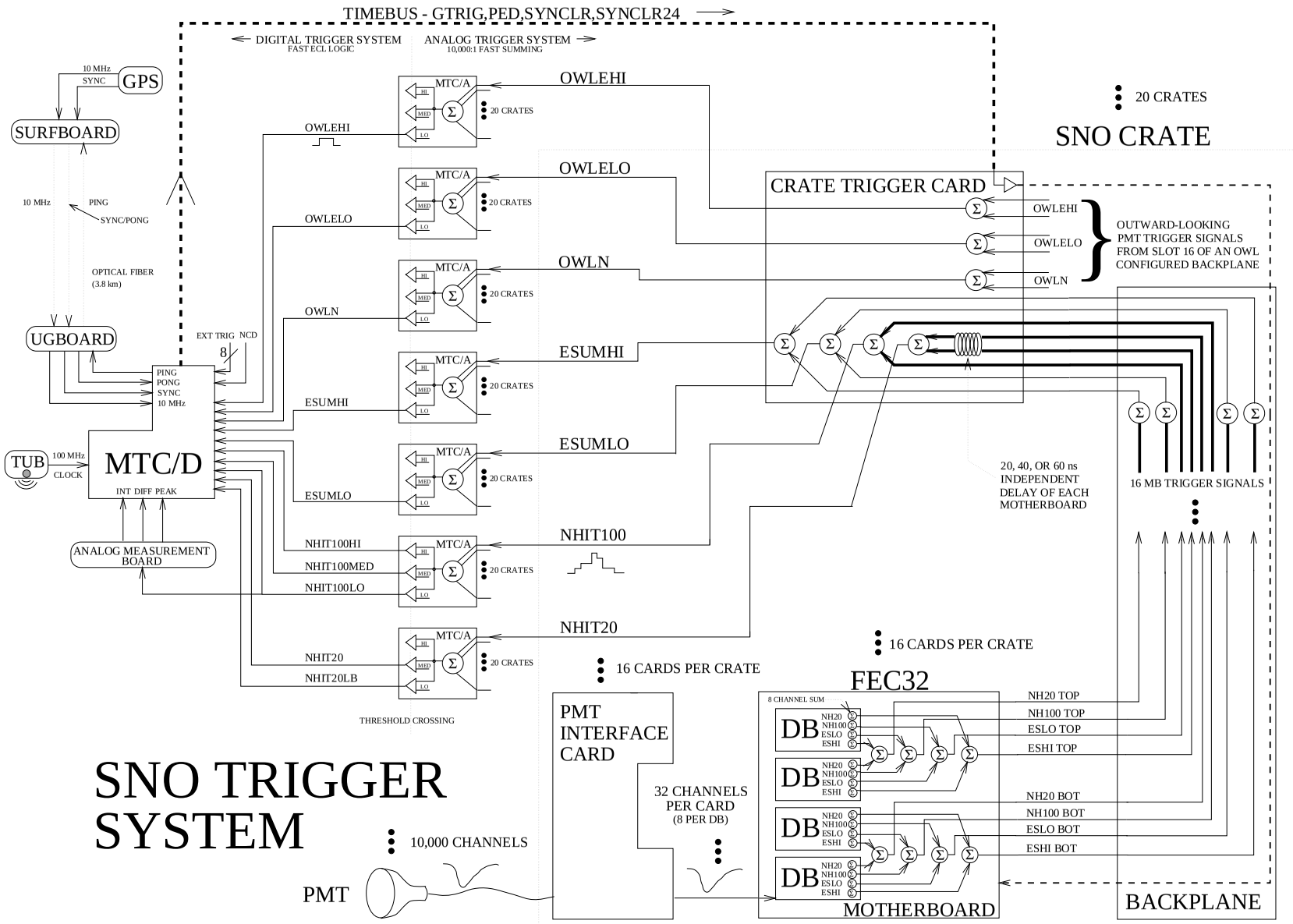


Figure 1: Block diagram of the the entire SNO trigger System

on to the crate-wide sum, and also carries the trigger timing control signals like the global trigger (collectively known as 'TIMEBUS' signals) to each of the Front End Cards. There are roughly 20 of these in the full system, one per electronics crate.

- *Crate Trigger Card (CTC)*: Each CTC sums up all the analog signals in a crate, and drives them on toward the central sum. It also acts as a receiver and fanout for the TIMEBUS signals. Like the BP's, there are roughly 20 CTC's in the full system.

- *Master Trigger Card/Analog (MTC/A)*: The MTC/A takes the sums from each CTC and sums them with all the others, and then determines whether that sum is large enough to exceed the currently set NHIT threshold. The full system has seven MTC/A's.

- *Master Trigger Card/Digital (MTC/D)*: The MTC/D handles all the digital logic for the trigger system, including the recording of trigger information like global trigger ID, the time of an event, and the fanout of all TIMEBUS signals.

- *Trigger Utility Board (TUB)*: Provides the master clock for the trigger system, as well as many utilities and diagnostics that interface to the MTC/D.

- *Surfboard/UGboard*: These are boards which provide the fiber optic interfaces to the GPS system, including the logic used to perform measurements of the surface to underground delay of the GPS signals.

- *Analog Measurement Board (AMB)*: This board provides diagnostics about the analog sums (derivative, peak, integral) which are digitized and passed into the data stream.

- *GPS Receiver*: A commercially built instrument which provides a clock and synchronization pulses from the Global Positioning Satellites.

2.1 Analog Summing

The choice of an analog trigger for the front end has several advantages. The first is speed—for the SNO trigger the time from tube N firing (for a threshold set at N tubes) to the time the corresponding global trigger is generated and returned back to the front end is roughly 240 ns, a time that is dominated by the cable lengths between the front end crates and the

central trigger electronics. Second, an analog system is naturally asynchronous, allowing a trigger to occur as soon as the Nth tube has fired with zero system dead time. In terms of the number of components and connections needed, an analog system is also far simpler than its digital counterpart. For example, the information describing how many of the 512 channels in a crate have been hit can be carried on a single cable from the crate to the central summing node. The reduced number and simplicity of components also leads to a much lower cost per channel.

An analog system does present its own problems, of course. For example, analog lines can be sensitive to electronic pickup which can contaminate the trigger sum. In the case of the SNO trigger, synchronous, detector wide, pickup at the channel level of just 20 μV can lead to a summed pulse equivalent in height to 100 tubes firing. Even at the FEC level, pickup of less than 1 mV per FEC can generate signals in a crate-wide sum larger than the trigger signals themselves (albeit with very different time characteristics). Eliminating all pickup at this level is not practical in a system so large, and therefore some events with fewer tubes firing than the desired threshold will still cause triggers when a pickup induced signal coincides with an analog sum close to threshold.

In addition, the analog pulse shape becomes a factor in the trigger efficiency. Figure 2 illustrates the difference in efficiency for the coincidence between two ideal and two real analog pulses, due to non-zero rise and fall times. As the diagram shows, when the two pulses are nearly out of time with each other, the finite slope for the edges produces a sum which is less than NHIT=2. Differences in pulse height and pulse shape from channel-to-channel can cause similar efficiency losses. (On the other hand, being able to vary pulse shape means that in principle one could design a trigger system that weights the coincidence window in some convenient way to *enhance* efficiency).

For SNO, the variation in efficiency with pulse shape can mean a variation in efficiency with event position. For example, events occuring near the PMT's themselves will have a different coincidence profile than events occuring near the center of the detector, and hence can require a slightly different threshold to produce a trigger for the same number of hit PMT's. One of the challenges then for the trigger system is to preserve as fast a rise and fall time as possible, even for single trigger pulses which originate in a single channel and must travel all the way from the front end electronics to the central summing node. A fast rise

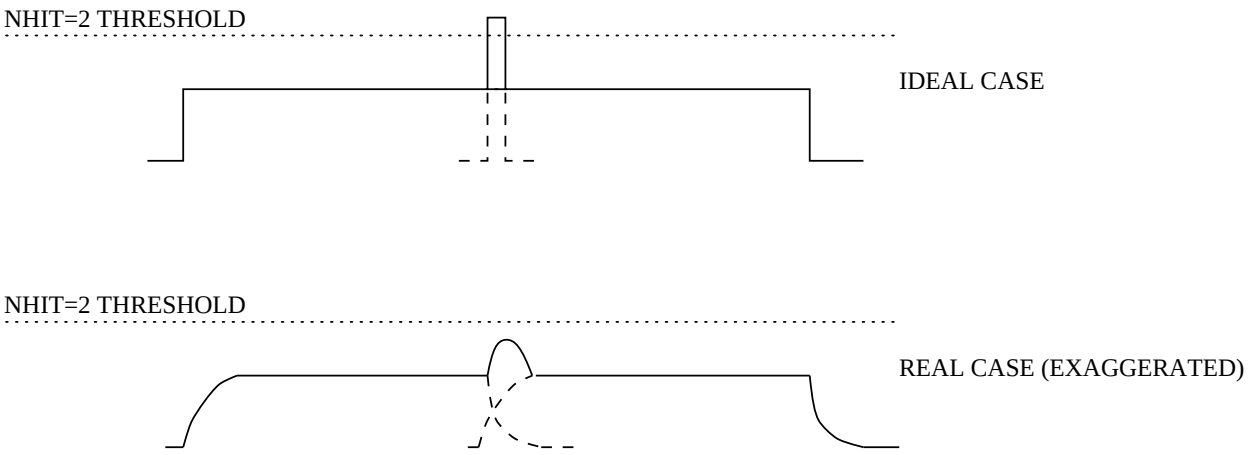


Figure 2: Exaggerated diagram of the effects of analog pulse shape on trigger efficiency. In the Figure, a threshold set at NHIT=2 triggers for ideal pulses, but not for those with finite rise and fall times.

and fall time also means that the trigger will be a good timing marker for each event.

As shown in Figure 1, there are several possible types of signal originating in the front end electronics which can be used to form a trigger sum and generate a trigger. They are:

- NHIT100 — A discrete pulse (uniform height for each tube hit) nominally 100 ns wide (the width is programmable over a narrow range whose maximum is near 100 ns). This is the nominal trigger we expect to use to take SNO data.

- NHIT20 — A discrete pulse nominally 20 ns wide (the width is programmable with a maximum near 50 ns). These pulses can also be delayed channel-by-channel to move the position of in-time coincidence to different locations in the detector. The main function of this trigger is for the study of backgrounds in the center of the detector.

- ESUMHI — A pulse that can take on a continuum of sizes, essentially a copy of the PMT pulse itself. Although the shape of the pulse precludes their use in a high efficiency, good timing trigger, they can be useful as diagnostics or for the construction of more complex trigger criteria (either on or off-line).

- ESUMLO — A low-gain version of ESUMHI.

- OWLN — An NHIT100 signal originating in an outward looking tube channel, and summed independently from the normal (inward looking) NHIT100 pulses.
- OWLEHI — ESUMHI from an outward looking tube channel.
- OWLELO — ESUMLO from an outward looking tube channel.

Each of these signal types are summed independently of the others, and as shown in Figure 1 and described in Section 2, the summing is done hierarchically. Eight channels on each SNO Daughterboard are summed, then the signals from each pair of DB's are summed on the MB and driven on to the SNO backplane (the signals from the DB's near the bottom of the backplane are kept separate from those on the top to minimize pickup from the lines of the SNO data bus). The FEC signals are then summed on the CTC, and that sum over all 512 channels in a crate for each trigger signal type is passed on to the MTC/A's where it is summed with the signals from the nineteen other crates.

The dynamic range of the trigger sum is limited ultimately by the total amount of current that can flow through each summing stage. Without any limits, the 300μA trickle of current that each channel puts out would become a 6 A torrent by the time it reached the last stage of summing if all channels fired simultaneously. The crate level summing stage on the CTC can accomodate all the current from the entire crate firing, but at the MTC/A the current is limited to two crate's worth. In addition to this limit, the final threshold comparator is nominally set to saturate at a limit of roughly 300 tubes, although this can be adjusted if necessary.

Each MTC/A can provide up to three separate trigger thresholds simultaneously, though the design currently calls for only one (the one summing the NHIT100 lines) to use all three. The trigger signals associated with the separate threshold crossings can all be fed in to the MTC/D where a decision is made as to whether any of them are currently considered a valid trigger.

2.2 Digital Trigger Logic

The digital half of the trigger system begins (and for the most part, ends) with the MTC/D. The MTC/D takes candidate trigger signals from the MTC/A's, and, if any of them are currently valid, it generates a global trigger which is sent out to the rest of the electronics.

In addition to the threshold crossing signals from the MTC/A's, trigger signals can be generated by the MTC/D itself or can be input from sources completely external to the trigger system. The MTC/D therefore plays three basic roles—the arbiter of valid triggers, a calibration source for the electronics, and a 'user interface' to the rest of the electronics for detector calibration sources.

The global trigger generation by the MTC/D is done by a continuous comparison of candidate trigger signals to the bits of a DAQ-programmable mask. If a trigger signal whose mask bit is enabled fires, a 'raw trigger' is created which is then synchronized to the MTC/D 50 MHz master clock and fanned out as the global trigger to all the electronics crates. All other trigger signals (there are up to 26 different types, see Section 8) which fire in coincidence with the signal initiating the global trigger will set bits in a trigger word which is saved as part of the trigger data bundle. In addition to the trigger word, with each event the MTC/D saves the count in the 50 MHz clock for use in analysis of inter-event timing, it saves a) the count in the 10 MHz clock for the recording of absolute (GPS) time, b) the current count in the global trigger counter for associating the trigger data with the front end PMT data, and d) several error and status flags. The MTC/D can store up to one million events in its on-board memory, and is capable of handling burst rates (for example, in the event of a nearby supernova) in excess of 2 MHz (continuous rates are limited by the speed of readout by the data acquisition system). Expected trigger rates for thresholds set at NHIT=20 are less than 1 kHz. Global trigger counts for every channel in the experiment are kept synchronized by pulses sent out by the MTC/D on every 16-bit and 24-bit rollover of the GT counter.

Calibration and monitoring of the electronics involves measurement of the slopes of the FEC32's ADC response to varying amounts of input charge (or time delay of signals relative to global trigger) and the determination of the absolute offset in the measurement of integrated charge (the pedestal). The slope of the charge response is done by injecting different amounts of charge into the front end (from the PMT Interface Card), the slope of the time response by firing the SNO discriminator at varying times relative to global trigger, and the measurement of the pedestal by forcing the discriminator to fire in the absence of input charge. The MTC/D provides a generator of pulses which can be sent at a fixed delay relative to the global trigger for measurement of the time slopes, and which has a programmable

width for the injection of different values of charge for measurement of charge slopes. These same pulses are used to fire the discriminators for measurements of the charge pedestal. The two synchronization pulses, the global trigger, and the calibration pulses ('pedestal' pulses) comprise the TIMEBUS which is fanned out to every SNO electronics crate.

In addition to the physics trigger signals from the MTC/A's and the on-board generated signals, the MTC/D can take up to eight trigger signals from any external source. All but one of these is synchronized to the 50 MHz clock as is any other trigger. While the synchronization provides simplictly of digital design as well as an extremely precise marker for inter-event timing, it does mean that the position of the in-time tubes in the acceptance window for each event will vary by up to 20 ns event to event. For most SNO analysis, this is unimportant since any differing offset between events can be removed after reconstruction. However, for some calibrations (for example, measurement of PMT timing) it is preferable to add the distributions from many events together without any resort to offline reconstruction (which, of course, depends on the calibration of PMT timing). The MTC/D accomodates this by providing one asynchronous external trigger input which produces a global trigger immediately, without regard to the state of the 50 MHz clock.

2.3 The Trigger Cycle

The trigger cycle begins with the firing of the SNO discriminators in response to either charge input above threshold (from a PMT, for example) or from a forced firing from the application of a pedestal measurement pulse. As shown in Figure 3 which details the trigger signals on the Daughterboard, the pulse from the SNO discriminator (called 'RESET') triggers the active channel's QUSN7 chip (SNO 'CMOS' chip) to spit out two small current pulses, the NHIT100 and the NHIT20 trigger signals, which are independently summed with the other seven channels on the DB. In addition, each of the SNO integrators on a DB sum the PMT pulses among four channels and present separate high and low gain current mode outputs for use as the ESUMHI and ESUMLO trigger signals. The signals output by each integrator are then summed with the corresponding sum-of-four signals from the other integrators on the same DB. The leading edge of RESET starts the timing cycle in the CMOS chips, a cycle which is stopped by the return of the global trigger if enough tubes have fired, or a timeout referred to as GTVALID.

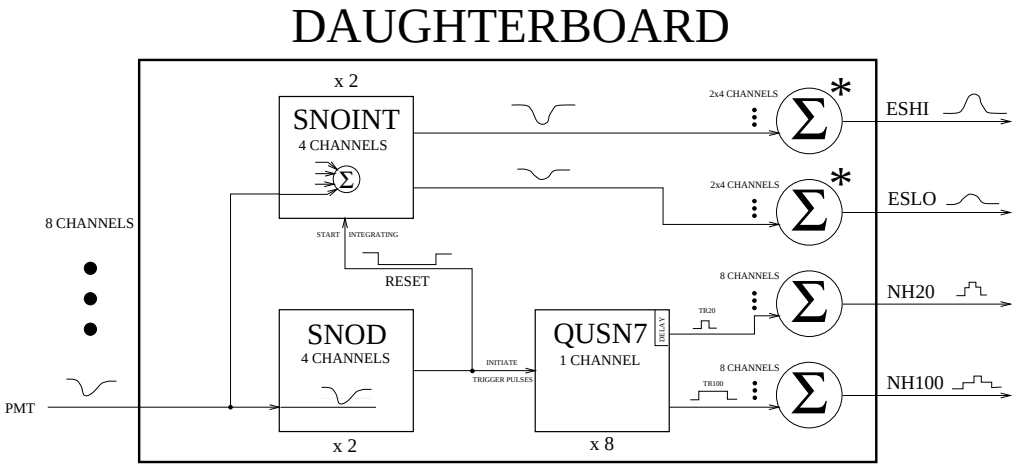


Figure 3: Block diagram of Daughterboard Trigger Path.

As described earlier, the trigger signals on each DB are summed on the Motherboards, driven on to the backplane and received and summed with the signals from other FECs on the Crate Trigger Card. From the CTC, the crate-wide sums are then sent off to the MTC/A's (one MTC/A for each of the seven trigger signals that can be sent from a crate) where they are summed with the signals from all other crates and compared with up to three different NHIT or ESUM thresholds. The time from the firing of the CMOS chip's trigger signals to to the threshold comparison on the MTC/A is roughly 95 ns, dominated by the 74 ns cable delay from each crate to the MTC/A's.

Once a trigger signal has crossed threshold, the MTC/A's comparator fires and a 20 ns logical trigger pulse is sent to the MTC/D. If the bit in the trigger mask corresponding to the firing signal is set, a 20 ns long 'raw trigger' pulse is created which then waits at a latch for the next tick of the 50 MHz clock. On the rising edge of the next 50 MHz tick, the raw trigger is latched and the global trigger is created and immediately sent back out to the SNO electronics crates to be received by the CTC's, driven on to the backplane, received by the FEC's and sent to the CMOS chips which, if they have data which has not timed out, store the time and charge information for their PMT. The total time from the firing of the Nth CMOS chip (for a threshold of N) to the return of the global trigger to that chip is roughly 240 ns, including the up to 20 ns delay due to the 50 MHz latch.

When the global trigger is created on the MTC/D, an additional signal called LOCKOUT prevents any other signal from creating a global trigger while the current trigger cycle is

active. LOCKOUT is expected to be set to 400-420 ns, during which time the MTC/D latches all of its trigger-related information and writes it to its on-board memory. At the end of LOCKOUT, if any trigger signal is still above threshold, a new global trigger will be generated immediately. Otherwise the system waits for the next threshold crossing or external trigger signal to start the cycle again.

3 Daughterboard Trigger Sum

The analog trigger sum begins on the Daughterboards, where eight channels of trigger pulses are linearly summed and passed on to more summing circuitry on the Motherboards. There are four different types of analog trigger signals on each DB, and each type is summed independently of the others. Two of the signals ('NHIT') are discrete, containing a fixed amount of current for each hit phototube, and two are continuous (energy sum or ESUM) with a current proportional to the charge seen in each phototube.

For the NHIT signals, a trigger cycle begins when the SNOD discriminator fires, in turn causing the CMOS chip to send out two small pulses of current (about 300 μA), one for each of the NHIT triggers. The width of the current pulses for each trigger can be varied digitally through settings in the CMOS shift register. The two different NHIT triggers differ mainly in their nominal pulse widths: NHIT100 referring to the signal nominally to be set near a 100 ns width, and the NHIT20 set at a tighter 20 ns. In addition, the NHIT20 signal can be programmed with individual channel-to-channel delays, to vary the position of the in-time triggers. The NHIT100 and NHIT20 trigger signals are each handled by identical circuitry external to the CMOS chips. The measured range of widths for the NHIT100 trigger is 10 ns to 93 ns; for the NHIT20 width it is 7 ns to 47 ns and for the NHIT20 delay it is 0 ns to 20 ns, all with channel-to-channel differences of up to 5 ns. Additional delays are added to the NHIT20 signal at the crate level to allow the position of the in-time light to be moved out toward the phototubes. Either or both of the NHIT signals can be disabled by unsetting their respective mask bits in the CMOS shift register. Appendix 1 describes the mapping of shift register bits to trigger pulse widths, masks, and delays.

The trigger signals from eight CMOS chips are summed on each DB using a high frequency NPN transistor in a common-base configuration as shown in Figure 4 (only the NHIT100

sum is shown; NHIT20 is identical). This common-base configuration is the basic building block of the entire analog trigger system, and is used alternately as a summing node (as in the Figure), an active termination, or as a current source. As shown in the Figure, for the DB sum, series resistors at the output of each CMOS chip are used to buffer each signal from the capacitance seen by the others. The transistors are biased by a single current source (one for NHIT100 and one for NHIT20) located on the Crate Trigger Card which feeds all the DBs in a crate (see Section 6). The bias for the summing transistor on each DB is roughly 1.5 mA. The base reference from the common base stage on the DB comes from a voltage divider, tuned to about 3.3 V. This voltage was found to reduce significantly overshoot in the current pulse produced by the CMOS chip.

The NHIT100 trigger lines are routed on the board from the CMOS chips to the summing transistors using traces as short as possible to minimize capacitance, and the CMOS chips on the DB are arranged mirror symmetrically to ensure that the summing transistor can be placed in the center of the chip configuration. Each trace is also shielded with short ground bands and travels above a low impedance ground or power plane, minimizing pickup from the TTL level signals used by the CMOS chip. Pickup conducted in from the backplane on the input bias current line is suppressed by using a very long time constant T-filter—2 series 3.5k resistors with a 0.1 μF capacitor in parallel. The transistor base is also heavily filtered with a 0.47 μF capacitor between two 50 Ohm resistors.

Nevertheless, some pickup from CMOS chip switching can be seen on the NHIT100 lines from the RDSTRB and CHIP_SELECT signals. The former has been demonstrated to be sourced from switching inside the CMOS chip itself, and appears at about the 1/5 NHIT level. The crosstalk from CHIP_SELECT (about 1/4 NHIT) is likely to be capacitive pickup due to the fact that the NHIT100 trigger output pin from the CMOS chip is adjacent to the CHIP_SELECT input pin. These signals are asynchronous and in worst case will present a slight shift in baseline.

The NHIT20 signals from the CMOS chips have significantly longer traces but are also surrounded by ground banding. The current sum has the same level of filtering on the input bias and base reference as does the NHIT100 current sum. There is much less pickup on the NHIT20 lines from digital switching near or in the CMOS chips, because of the somewhat better geographical location of the output pin on the CMOS chip.

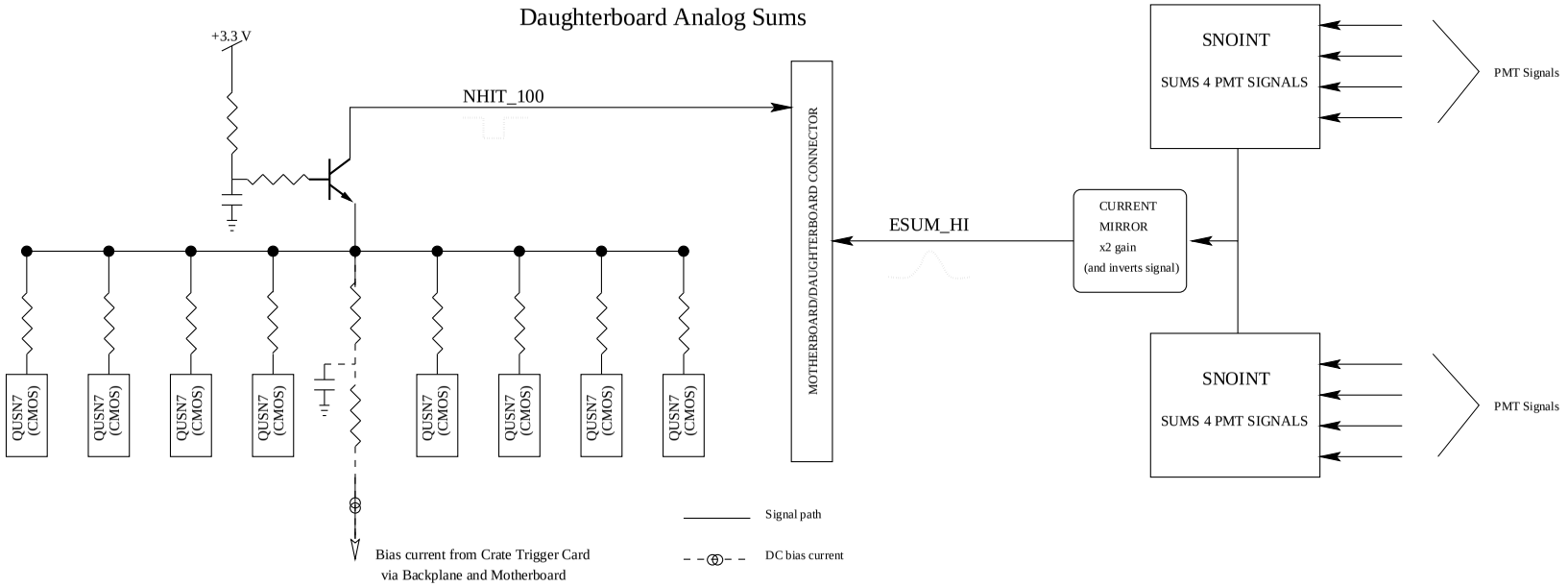


Figure 4: Daughterboard Analog Sum Circuits. Only NHIT100 and ESUMHI are shown.

The ESUM trigger signals are handled somewhat differently. The two independent signals are essentially PMT pulses passed through the integrator with some shaping and small delays. The signals differ only in their respective gains, ESUMLO being roughly a factor of 16 lower than ESUMHI. Each integrator yields the sum of four channels as shown in Figure 4 for the ESUMHI signals, and the two integrator signals are summed in a PNP current mirror with two output stages tied together to provide roughly a factor of two in gain with very few components. The bias current is provided by the integrator itself, roughly 2 mA per DB. The current mirror used to provide the factor of two gain also means that the ESUM signals are inverted relative to the NHIT signals as they leave the DB.

4 Motherboard Trigger Sums

On the Motherboard, the summed NHIT signals from each of the Daughterboards are summed again in two pairs, one for the two DB's nearer the bottom of the crate and one for the two nearer the top, as shown in Figure 5. This second stage of summing is done again through a common-base NPN stage, with a series resistor near the summing node to help isolate each signal path. The bases of the summing transistors are referenced to +8 V, ensuring that even if all 16 channels in the sum fire, the DB transistors are well away from saturation. Each sum of 16 CMOS channels is fed out onto the backplane on a line dedicated to the trigger signals for that particular FEC (one on the top side of the backplane, one on the bottom).

The output of the ESUM current mirrors on each DB are summed in pairs similarly to the NHIT signals, one for the bottom two DB's and one for the top two, again as shown in Figure 5. The second stage of summing is a parallel pair of PNP's in the same type of common base configuration used for the NHIT signals. Before leaving the FEC, the bias current supplied by the integrators is subtracted through large parallel resistance to -15 V, to bring the DC current close to zero on the backplane. This allows the trigger sum to operate normally with cards removed.

To minimize capacitance, all trigger signals are routed on the surface of the MB. The signals are routed above low impedance ground planes in isolated, analog regions of the MB, to reduce pickup from the digital switching. The ground plane itself is notched to prevent

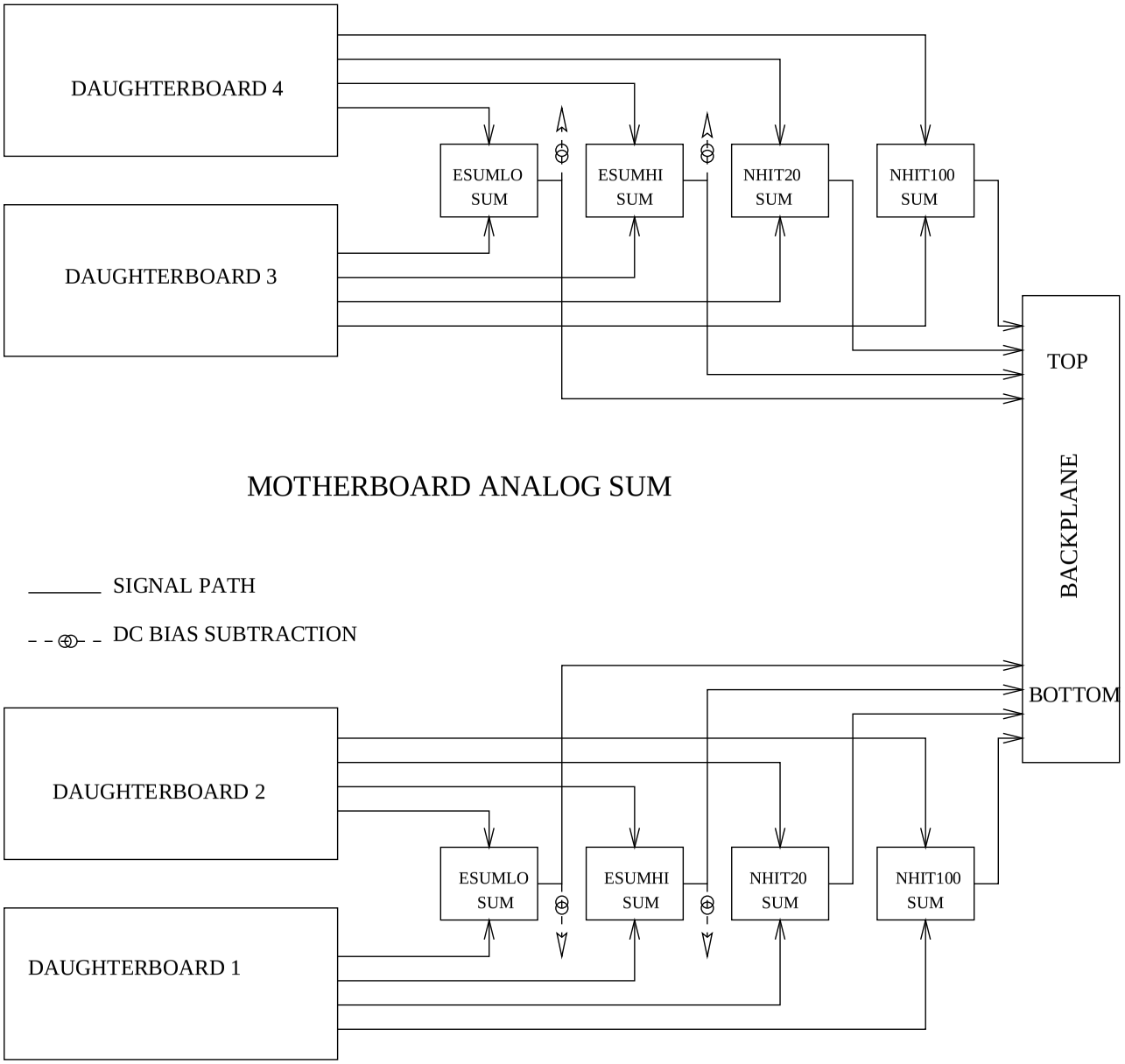


Figure 5: Block diagram of Motherboard trigger sum.

ground currents associated with the digital processes from flowing underneath the trigger lines, and in addition the traces are guarded with ground banding for nearly their full length. The characteristic impedance of the traces on the surface of the board has been tuned to $\sim 75\Omega$.

5 SNO Backplane Trigger Handling

Each of signals for the NHIT trigger sums leaving a FEC travels on independent backplane lines and is terminated on the Crate Trigger Card (CTC). The traces for the NHIT100 sum are on the FEC side (front) of the backplane (16 signals on the top, 16 on the bottom) and the traces for the NHIT20 sum are on the PMT Interface Card side (back). Each trace is surrounded by ground bands connected at both ends to the backplane ground plane, to minimize crosstalk between the signals. To minimize pickup from the GTL and ECL lines used to communicate to the FECs, the NHIT signals are routed as far as possible from the FEC backplane connectors.

The slower rise time and looser timing requirements for the ESUM triggers allows the signals from each pair of Daughterboards to be summed on a backplane line common to all FEC's, which ends in an active termination on the CTC. Although the ESUM signals are routed through the FEC backplane connectors (and hence near the data and address lines), they are shielded by ground pins on the connectors.

FEC slot 16 differs from other backplane slots since it can be filled by a FEC dedicated to outward-looking (OWL) tubes. To accomodate an OWL tube FEC, sets of jumpers on the backplane can be hard-wired to disconnect the trigger signals from the normal backplane lines and connect them to special signal paths used only by OWL tube circuitry. For the OWL tubes, only the NHIT100 and ESUM triggers are implemented; the NHIT20 trigger is disconnected by removing the jumper connecting the slot 16 FEC to the usual NHIT20 trigger lines. In addition to jumpers for the signal paths, the backplane also has jumpers for the bias current provided by the CTC for the OWL tube circuitry. With an OWL tube FEC in slot 16, the jumper connecting the bias current for the NHIT20 sum on the slot 16 DB is removed, since the NHIT20 lines for that FEC will not be connected to the CTC. Backplane jumpers then need to be connected to feed bias current for OWL circuitry on the CTC (see

Section 6). Appendix D details the explicit jumper connections for normal and OWL tube running.

Initial tests of the backplane found pickup on individual NHIT trigger lines due to backplane switching at a level equivalent to 1/4 of a single NHIT100 pulse ($\sim$ 4 mV on the backplane lines). Although this level by itself was not significant, the fact that the lines are summed (32 total for each NHIT trigger) meant that the total pickup for a full crate could exceed a level equivalent to NHIT=8 (albeit with narrower timing characteristics than the trigger signals themselves). The problem was found to be the power plane carrying the termination voltage for the GTL backplane signals. This plane was directly underneath some of the trigger lines, and despite its low impedance and multiple local bypasses to ground, it carried significant voltage and current spikes which caused the pickup on the trigger lines. The solution to the problem was to move the GTL termination voltage to an external line soldered to the backplane, and to connect the former GTL termination plane to the other ground planes on the board using wide strips of copper. The expected level of pickup now with a full crate averages less than 1/2 of a single NHIT100 pulse though small spikes can individually exceed NHIT=2. The grounding of the former GTL plane also reduced a small amount of pickup from the clock lines traveling on the backplane, reducing that to less than NHIT/5 for a full crate.

6 Crate Trigger Card

The main function of the Crate Trigger Card (CTC) is to sum all of the 512 trigger signals in a crate and pass that sum on to the central sum over all 20 crates done on the Master Trigger Card/Analog (MTC/A). In addition, the CTC supplies bias current for the NHIT sums for the Daughterboards in the crate, adds programmable delays to the NHIT20 signals, receives and passes on to the backplane the TIMEBUS signals from the MTC/D (GTRIG, PED, SYNCLR, and SYNCLR24), and also provides external inputs for testing a crate in 'standalone mode', that is, unconnected to the Master Trigger Cards. Figure 6 is a block diagram summarizing the functionality of the CTC.

The trigger signals summed by the CTC are:

1 **NHIT100**: 100 ns trigger sums from each Motherboard (32 signals)

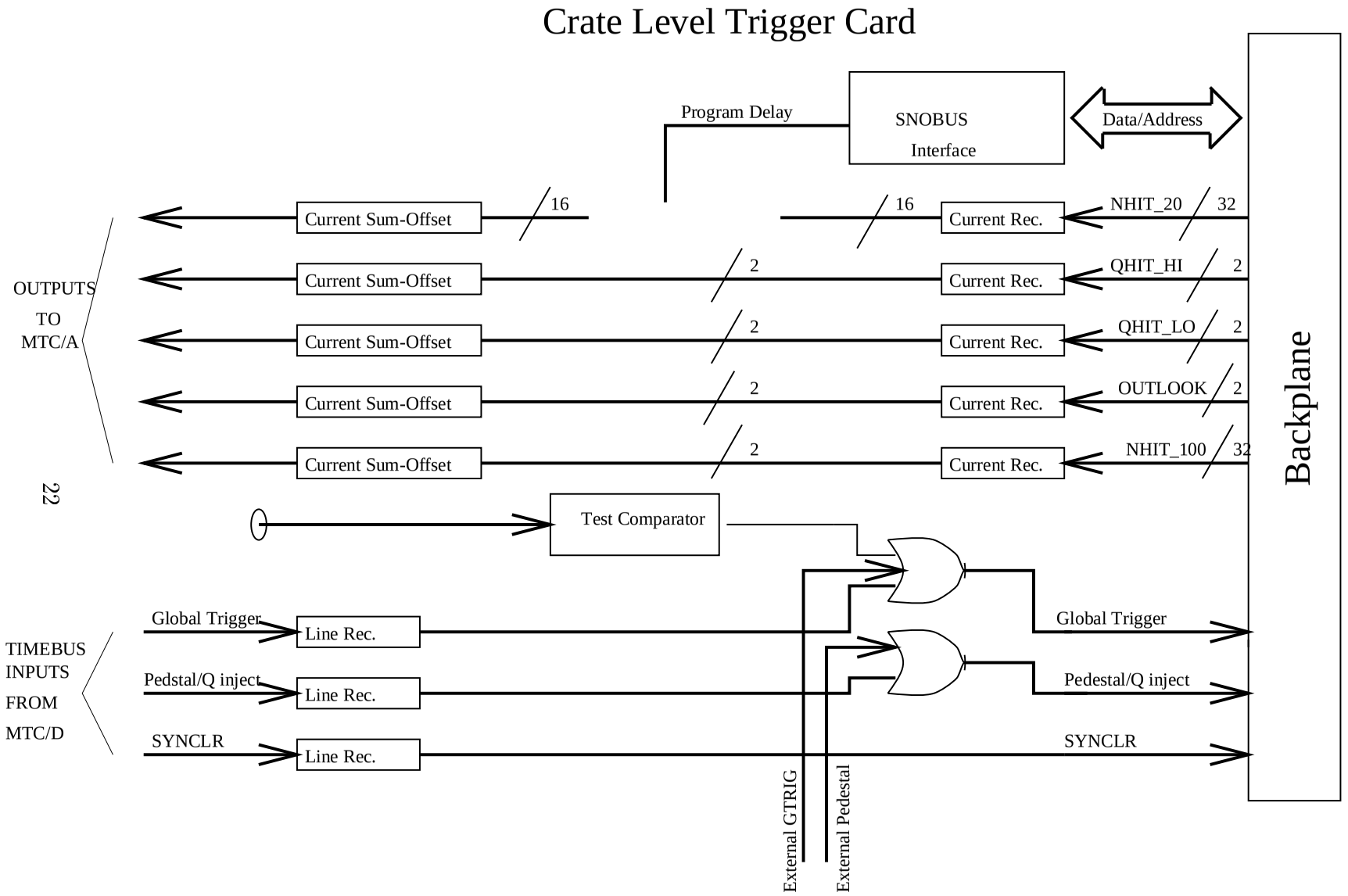


Figure 6: Block diagram of Crate Trigger Card Functionality.

2 **NHIT20**: 20 ns trigger sums from each Motherboard (32 signals)

3 **ESUMHI**: High gain energy sums from each Motherboard (32 signals)

4 **ESUMLO**: Low gain energy sums from each Motherboard (32 signals)

5 **OWLN**: Outward-looking tube NHIT sum from slot 16 Motherboard (2 signals, if OWL FEC is present)

6 **OWLEHI**: Outward-looking tube ESUMHI from slot 16 Motherboard (2 signals, if OWL FEC is present)

7 **OWLELO**: Outward-looking tube ESUMLO from slot 16 Motherboard (2 signals, if OWL FEC is present)

As shown in Figure 6, these signals are all handled in much the same way—they are terminated after coming off of the backplane, then summed and driven out by a current mirror after having their DC bias current subtracted off. The exception is the 20 ns trigger signal line, which also has programmable delays implemented with relays and off-board delay lines.

6.1 NHIT100 Analog Sum

There are four main components to the NHIT100 analog sum on the CTC, as shown in Figure 6.1:

- *Active terminations*: 32 active terminations of the trigger signals coming off of the backplane (16 for the signals coming off of the top half of the backlplane, and 16 for the signals from the bottom half).
- *Summing node*: A common-base summing stage for each set of 16 signals (one for the top of backplane signals, and one for the bottom)
- *Biasing and subtraction current mirror*: Used both to source current to all the DB'S in a crate and to generate copies used to subtract DC current from the output of the CTC for a net zero current flowing into the MTC/A.

- *Output current mirror*: Inverts sum of both summing nodes so output can be referenced to ground. Also has built-in gain of two.

The active terminations of NHIT100 sum on the CTC are very much like the summing done on the DB's and MB's—they are common-base configured NPN's. Each termination handles one signal from the backplane, and as described in Section 5, each backplane signal is a sum of 16 CMOS channels (two DB's). The termination impedance is roughly matched to the 75Ω characteristic impedance of the backplane with a 68.1Ω series resistance in the emitter of each of the common-base NPN's (the small resistance looking into the emitter accounts for the rest of the 75Ω). The base reference for the common-base NPN's on the CTC is 10 V, ensuring that even if all 16 channels feeding a particular termination fire, the MB summing node on the other end of the backplane signal stays well away from saturation. The terminations are arranged in two sets of 16, reflecting the vertical division of the two halves of the backplane, and the traces are routed to the terminations 'inside out'—the trace from the FEC closest to the CTC travels furthest—in order to partially cancel the differential delays due to FEC position on the backplane.

The bias current for each of the CTC's NHIT100 active terminations comes from the summed bias current of the pair of DB's feeding that particular line. The original source of this current (about 1.5-2.0 mA per DB) is a stiff current mirror on the CTC itself. As described in Section 3, the current from the CTC is fed out onto the backplane and the summing transistor on each DB taps off its 1.5 mA worth. As described below, this same CTC current mirror is used to generate subtraction currents in fixed ratios of the initial sourced bias current, ensuring that no DC current flows out of the CTC and on into the MTC/A. The use of the single current mirror to generate both the source current and the subtraction current lowers the overall power budget of the trigger system and also provides a first order cancellation of drifts in DC level due to temperature and power supply changes.

After passing through the active terminations, the NHIT100 signals are summed by wiring all their collectors together and feeding them into another common-base stage. There are two copies of the summing common-base stage, one to sum the outputs of the terminations of the 16 signals from the top half of the backplane, the other for the outputs of the terminations of the 16 signals from the bottom. To minimize the capacitance seen by the signals entering this summing node, a series resistance of 300 Ω is used in the collector of each of the active

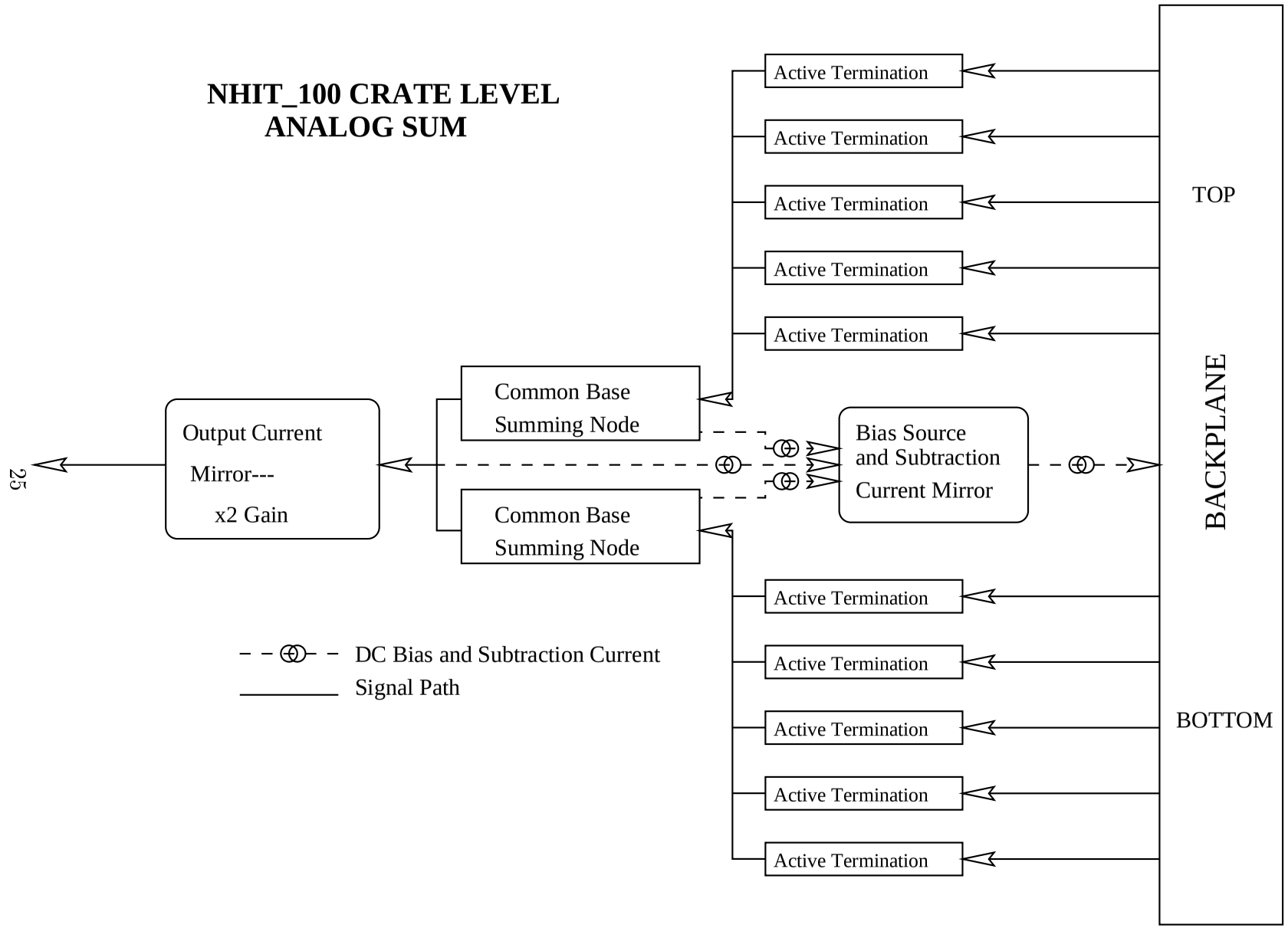


Figure 7: Block diagram of NHIT100 trigger sum.

terminations, and the trace connecting each set of 16 is as short as possible given the physical constraints of component size and placement.

The two common-base sums are each made from two parallel NPN's, allowing all 256 channels (= 16 FEC's x 2 DB/half FEC x 8 channels/DB) to fire without exceeding the maximum collector current of any single transistor. In addition, the base reference of the common-base stages is at 15 V, keeping the active terminations contributing to the sums away from saturation even when all channels fire simultaneously.

At this point, the DC bias current flowing into each of the common-base sums is half of all the current sourced out to the DB's—roughly 50 mA, too much for the rating of the transistors. The current is reduced by subtracting off 3/4 of the original source current before the sums enter the common-base transistors. The source of this subtraction current comes from an inverted copy of the same mirror used to generate the current sent out to the DB's. After the subtraction, the total current flowing in the system is $\sim$ 25 mA. For a detailed description of how the bias source and subtraction current is tuned, see Appendix E.

The two common-base summing stages have their collectors wired together, summing all the channels in a crate. The sum is then fed into a Wilson-configured PNP current mirror (with a gain of two), in order to reference the output signal to GND (and make it more amenable to scope measurements and measuring of DC offsets). To eliminate the DC current left over from the subtraction prior to the common-base summing stages, the remaining 1/2 of the original current (1/4 x gain of 2) is subtracted from the output signal before leaving the CTC. This subtraction is done through two parallel NPN's cascoded with a copied output from the original DB biasing current mirror. The sourcing of the output current from a Wilson current mirror and the subtraction of the leftover DC bias current through a cascode stage leaves a very stiff, 'floating' current source as the output of the CTC, virtually unaffected by differences in ground levels between the crates and the MTC/A. Because of the effects of finite beta, Early voltage, and the mismatching of the discrete transistors making up the biasing current mirror, large 'tuning' resistors are available for trimming the DC output current to ensure that it is close to zero. These resistors are referenced to +24 V on one side and tied to the emitters of the cascoded current subtraction on the other. Reducing the resistance between those two points reduces the amount of current subtracted from the output of the CTC. See Appendix E for the procedure for using these resistors to eliminate

any non-zero DC current in the CTC output.

The NHIT100 pulses leaving the CTC have rise and fall times of roughly 2 ns (with a full crate of FECs), as well as some overshoot left over from the overshoot produced by the CMOS chips themselves. The pickup from the clocks in the crate produces a fuzz of about 1/4 NHIT, as described in Section 5. Small drifts (rms of $\sim$2 mV) in the DC level can also be seen on the output, due to variations in the balancing of the biassed and subtracted current (due, presumably, to temperature variations). This drift can have excursions of up to 8 mV ($\sim$1/4 NHIT), corresponding to about 0.2% of the total current.

6.2 NHIT20 Analog Sum

The NHIT20 analog sum on the CTC differs from the NHIT100 only because of the addition of off-board delays. As described in Section 3, individual NHIT20 trigger signals can be delayed relative to one another, with the delay value specified through a shift register in each CMOS chip. As also described in Section 3, the maximum delay of 20 ns in the CMOS chip is too small to move the in-time trigger point far away from the center of the detector, and so additional delays were added on the CTC to increase the maximum to 80 ns. The idea for the additional delays is to allow all the channels on a given FEC to be delayed relative to those on the other FECs in discrete amounts, relying on the remaining channel-to-channel delays to come from the CMOS chips. For this to work, the mapping of positions of the PMT's on a given FEC must be such that the maximum relative delay from one channel to another on the same FEC never needs to be greater than 20 ns (the CMOS chip's maximum delay).

Figure 8 illustrates the six major components to the NHIT20 analog sum:

- *Active terminations*: 32 active terminations of the trigger signals coming off of the backplane (16 for the signals coming off of the top half of the backlplane, and 16 for the signals from the bottom half).

- *Delay register and relays*: Bits in the register switch trigger signals through four possible paths, each with a different relative delay (from 0 ns, 20 ns, 40ns and 60 ns).

- *Delay-specific summing nodes*: Four separate common-base summing nodes drive the signals through each of the delays. These nodes can sum from one to sixteen signals,

depending on how many are switched through a particular delay path.

- *Delay-specific terminations*: At the other end of the delay from the summing nodes, these terminations are nearly identical to the terminations of the signals from the backplane.

- *Biasing and subtraction current mirror*: This mirror is used both to source current to all the DB'S in a crate and to generate copies used to subtract DC current from the output of the CTC for a net zero current flowing into the MTC/A.

- *Output current mirror*: The output mirror inverts sum of delay specific terminations nodes so that the output can be referenced to ground. It Also has built-in gain of two.

The active terminations for the 20 ns trigger signals are identical for those of the NHIT100 signals—common-base configured NPN's with 68.1 Ω emitter resistors. The bias current for these comes from the original current sourced to the DB's, as is true for the NHIT100 signals. However, unlike the NHIT100 signals, the NHIT20 signals are first summed in pairs from common FECs, as shown in Figure 8. In other words, the signal from the top half of the backplane corresponding to one FEC is summed with the signal from the same FEC coming from the bottom half of the backplane, immediately after passing through their respective active terminations. The reason for this is that the delays are added on a FEC-by-FEC basis, and it is much more efficient to switch the signal for an entire FEC through its delay rather than do two separate switches for each half of the FEC.

The summed signal from each FEC then passes through the relays. As shown in Figure 8, there are three relays for the signal from each FEC, and each set of three is controlled by two bits in the delay register allowing four possible delays paths. The higher order bit of the two controls the first relay, choosing which of the next two relays to switch the current through. The lower order bit switches the chosen second relay between its two possible delay paths. Appendix C details the mapping of bits in the delay word to delays for the signals from each FEC.

All signals switched into a particular delay path are first summed in a common base stage like that used to sum the NHIT100 signals. Here, the common base stage is made of two NPN's, each one handling up to 8 sums from the FECs. Because it is not known how many signals may be entering a particular common-base summing node (one or more

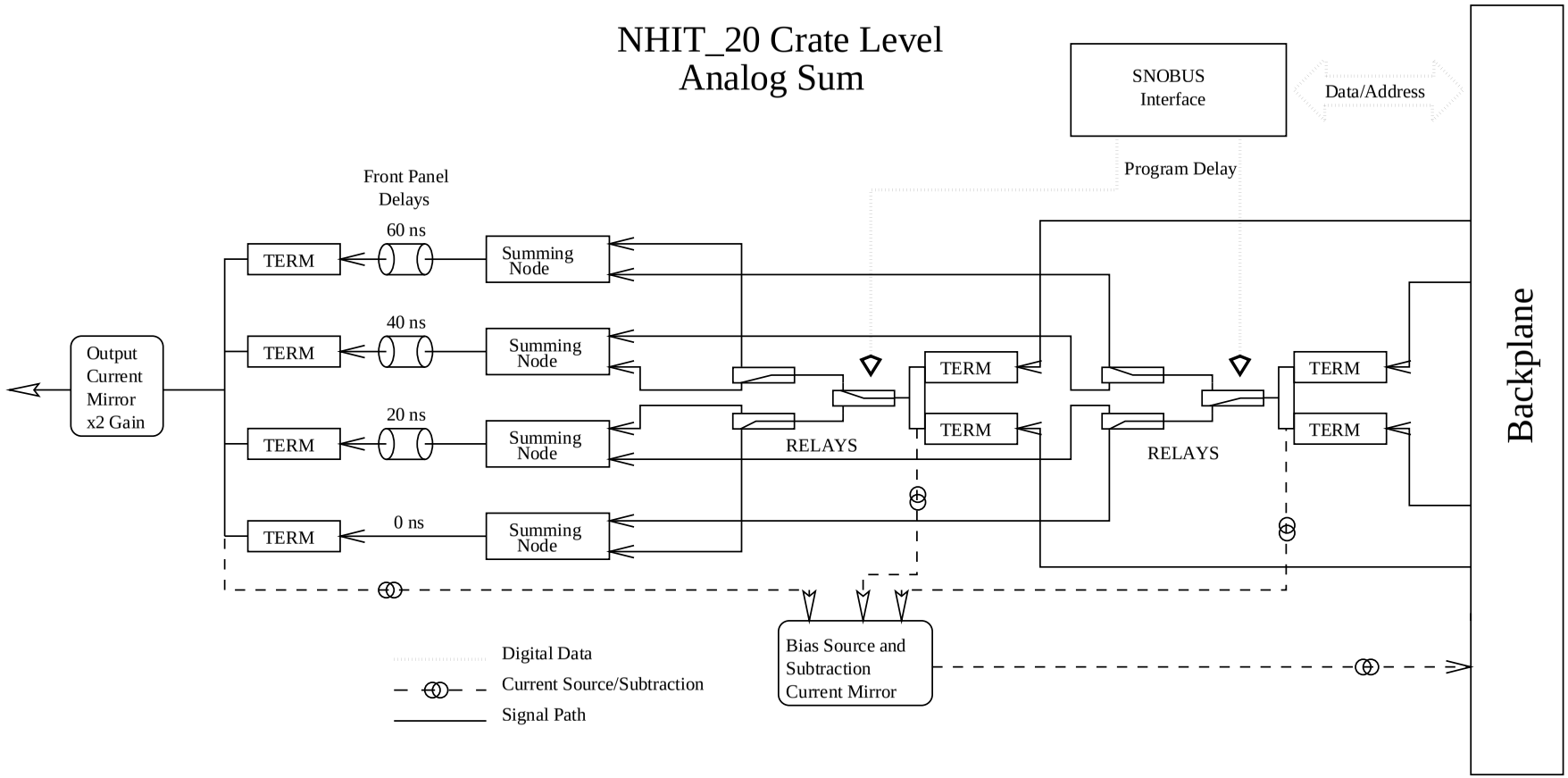


Figure 8: Block diagram of NHIT20 trigger sum. The sums for only two FEC's are shown.

may be switched out to take a different delay path), the first current subtraction for the NHIT20 signals must happen before the signals enter the relays. The subtraction current comes from a current mirror identical to that used for the NHIT100 trigger signals, but is now split sixteen ways to subtract a small amount from each FEC sum coming out of the active terminations. A 3kΩ resistor in series with the subtraction current for each FEC sum is used to buffer the signals from the large trace capacitance resulting from the sixteen-way split.

From the common base summing nodes, the signals are driven through their individual delays. The '0 ns' delay is implemented simply as trace on the CTC; the three others are cable delays external to the board. At the end of each of the delays are common-base active terminations like those used to terminate the FEC signals coming off of the backplane. The collectors of these terminations are joined together to sum up the signals from all of the different delay paths. After manufacture of the CTC's, it was found that this particular termination/sum was prone to oscillation, and base resistors were added to eliminate the problem.

The four tied collectors feed an output current mirror identical to that used for the NHIT100 trigger sum, and at the ouput of the mirror a final tuning subtraction is done in the same way using a copy of the current from the original biasing current mirror.

The NHIT20 pulses, having passed through more stages than the NHIT100 signals, do not have timing characteristics as quite as good, with rise and fall times of about 3 ns. The clock and Backplane pickup, however, is nearly negligible because the NHIT20 lines are on the back side of the Backplane, as described in Section 5.

6.3 Outward-looking Tube NHIT Sum

The outward-looking tube NHIT sum (OWLN) is simply a one-FEC version of the NHIT100 sum. In a crate containing an outward-looking tube FEC, jumpers are set on the backplane to route the NHIT100 trigger signals for the outward-looking tube FEC through the OWLN sum circuitry on the CTC (see Section 5). Backplane jumpers also route 1/16th of the normal NHIT100 bias current through the outward-looking tube FEC. The OWLN trigger signals are terminated on the CTC in the same way as the normal NHIT100 signals, and the signals from the top and bottom half of the backplane are summed through a common base

stage identical to that used for NHIT100. The final output current mirror is also the same design as that used for the NHIT100 and NHIT20 outputs.

Current subtraction is done at the common-base summing node and on the final output in an identical way as for the NHIT100 signals except for the magnitude (1/16th) of current used.

The lower amount of bias current used by the OWLN trigger gives it somewhat poorer timing characteristics than the general NHIT100 sum.

6.4 Energy Sums

There are four identical energy sum (ESUM) triggers on the CTC, two for the normal low and hi-gain energy sums originating in the integrators on the Daughterboards, and two low and high gain energy sums available for an outward-looking tube FEC (OWLE's).

Each of the ESUM trigger circuits on the CTC has only three major components, as Figure 9 shows:

- **Active terminations**: Two terminations of the ESUM lines coming off of the backplane, one for those coming off of the top half and one for those coming off of the bottom.
- **NPN current mirror**: Acts as a summing node for the outputs of the active terminations and also provides a gain of two.
- **Output current mirror**: Inverts and drives the current sum off the CTC.

The general construction of the ESUM trigger sums is similar to the NHIT trigger sums—common-base terminations on the inputs and inverting, gain-stage current mirrors on the output. The three major differences are that the backplane does not have separate lines for the sums coming off of each FEC, that the sense of the current for the ESUMs coming on to the CTC is inverted with respect to the NHITs (due to the initial inverting current mirror on the DB), and that the bias current for the DB's is not sourced by a current mirror on the CTC.

The absence of individual trigger lines for each FEC means that for each type of ESUM trigger signal, the backplane acts as a summing node. As described in Section 5, each ESUM

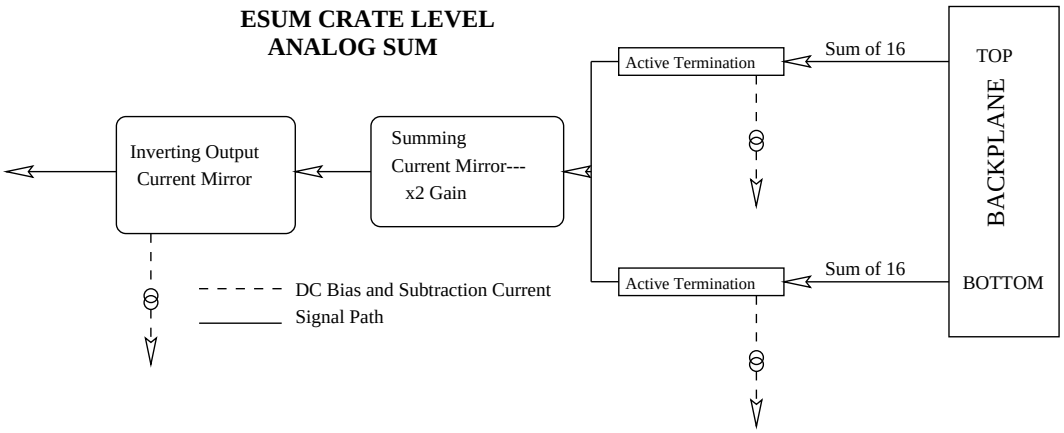


Figure 9: Block diagram of one of the ESUM trigger sums.

trigger type has one line for the sums coming from the DB at the top of the backplane, and one for those at the bottom. There are therefore only two common-base terminations for each ESUM trigger on the CTC for all of the FECs in a crate.

The terminations are built out of fast, high-current PNP's rather than the NPN's used for the NHIT triggers in order to handle the inverted current sense of the ESUM signals. The collectors of the terminations are wired together and fed into an NPN current mirror used to double the current and alter the reference to -24 V. The output of this mirror is fed into a PNP current mirror which inverts it again (giving it the same sense as the NHIT currents) and also provides a way of referencing the signal to ground while keeping far away from saturation.

The bias current for the ESUMS on the CTC come from large resistors pulled up to a +24 V power supply. These resistors provide about 4 mA of current for each termination. The bias is summed (as is the signal) and doubled by the first current mirror, resulting in an expected 16 mA total. After inversion by the final current mirror, the bias is subtracted through resistors pulled down to -24 V. However, because of the finite DC current sourced by the FECs (the current subtraction on the FEC's for the ESUMs is not perfect—see Section 4), the amount of current that needs to be subtracted is somewhat less than the full 16 mA. The resistor values for this final subtraction are therefore determined by the amount of current needed to cancel the leftover bias coming through final current mirror.

6.5 Test Comparator

A comparator is available on the CTC for triggering the crate in 'standalone' mode. The outputs of any of the triggers can be fed back into the 'test' input of the CTC, and if the CTC sum exceeds the comparator threshold, a local global trigger is created and sent out onto the backplane along the normal global trigger path. The local global trigger is initiated by the threshold crossing of the comparator, and is produced by an ECL flip-flop wired as a one-shot with a pulse width of ~500 ns. The comparator threshold can be set either by a trimpot soldered on to the board or by hardwiring in a pre-set threshold to each board.

6.6 Other Inputs

The CTC also receives the (differential ECL) TIMEBUS signals from the MTC/D (global trigger, pedestal, and the two synchronous CMOS counter clear signals) and drives them on to the backplane. The input is through a 10-pin connector mounted directly on the board, designed for a twisted-pair cable. The receivers and drivers are all MC10H116's with propagation delays of less than 2 ns each.

In addition, there are external pedestal and trigger inputs for use in testing the crate with an external pulser. These inputs are single-ended ECL inputs through BNC connectors on the front panel, and are wire-OR'd into the usual global trigger and pedestal signal paths.

7 Master Trigger Card/Analog

The purpose of the analog half of the Master Trigger Card —the MTC/A—is to sum all of the analog sums from each crate and determine whether that sum exceeds the programmed (NHIT or ESUM) threshold. Like the Crate Trigger Card, the MTC/A is a combination of common-base terminations, summing nodes, and current mirrors. In addition, the MTC/A has triggering logic (like the CTC's test comparator circuitry) which does the actual threshold comparison and allows retriggering at the end of a trigger cycle if the threshold is still exceeded by the analog sum. The MTC/A is simpler than the CTC in many ways, however, since there are no delays to control and since only one type of trigger is input to a given MTC/A. For a full system, 7 MTC/A's are required to handle the 7 trigger types discussed in Section 6.

Figure 10 illustrates the major components of the MTC/A:

- *Active terminations*: 20 active PNP terminations of the trigger signals coming from each CTC.
- *Summing nodes*: Four common-base summing nodes, each summing five CTC signals.
- *Cascoded current subtraction*: Used to subtract off a large fraction of the bias coming from the active terminations.
- *Overcurrent limit*: At two different stages, a diode clamp limits the total current flowing through the system to two full crates' worth.
- *Output current mirror*: Inverts sum of four summing nodes so output can be referenced to +5 V. Provides four copies of sum.
- *Comparator circuitry*: Three comparators with one-shots to provide 20 ns wide 'raw' trigger signals when analog sum crosses the threshold of each.
- *Retrigger circuitry*: Logic and one-shots to allow retrigger if analog sum is still above threshold at the end of a trigger cycle.
- *DAC interface*: Three DACs programmable by MTC/D to provide individual thresholds for each of the comparators.

7.1 Analog Design

The active terminations on the MTC/A once again employ simple common-base amplifiers, in this case PNP's to accomodate the CTCs' positive going signal currents. The bias for each of the terminations is sourced by a large resistor pulled up to +24V, providing about 8 mA for each of the 20 terminations. Since each CTC is capable of driving the current from the firing of an entire crate (about 300 mA), each termination on the MTC/A is physically constructed from two PNP's in parallel, in order to prevent the current rating of any one transistor from being exceeded.

The output of the terminations are summed in groups of five through yet one more (and final) common-base summing node. This common-base stage is again constructed from two

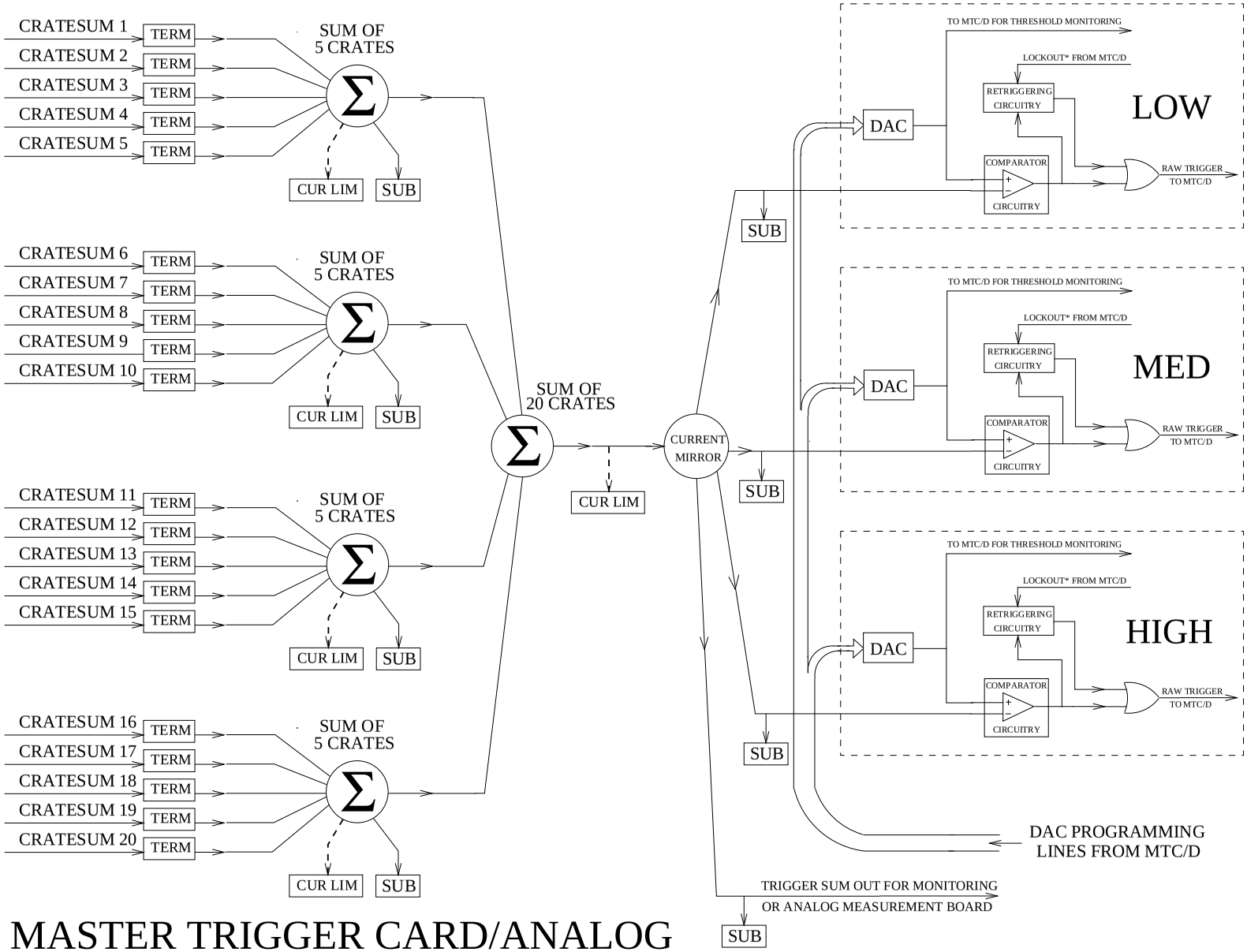


Figure 10: Block diagram of Master Trigger Card/Analog.

parallel PNP's to handle large currents. To prevent too much DC bias flowing through the summing stage and the rest of the system, a cascoded current source made of high current NPNs subtracts off roughly 35 out of the nominal 40 mA flowing in.

In addition to the subtraction of the DC bias before the summing node, a diode clamp acts to limit the maximum output pulse height. The diode is referenced with a 5 V zener, and conducts when the current exceeds roughly two crates' worth—600 mA. Without this overcurrent limit, the total current flowing when the entire detector fires would approach 6 A.

Once through the summing node, the signals from each set of five crates is summed by tying together the collectors of the four summing nodes through 10 Ohm series resistors. This sum, now over all channels in all crates (10000:1), is fed into a current mirror which produces four inverted copies of the input, one of which is driven off the board for monitoring purposes. A diode clamp limits the input to the current mirror to no more than two crates' worth of current. The majority of the remaining bias—about 20 mA—is subtracted off at the output of the current mirror through large resistor pull-ups to +24 V.

The current that is left over, unfortunately, is not a perfect constant. The output of the MTC/A analog section has both a low frequency 'bounce' and an even lower frequency drift (like that on the CTC's—see Section 6) that vary slightly the amount of current flowing out. The bounce looks spectrally very much like flicker or $1/f$ noise, and has a peak-to-peak amplitude of about 4 mV ($\sim$ NHIT/8) and an rms of 0.8 mV when taken across 50 Ohms (the nominal final load for the trigger sum). Although not completely understood, the bounce does seem to be related to the initial cascoded current subtraction done before each of the five-fold crate sums. The drift is somewhat more serious since it has a peak-to-peak amplitude between NHIT/4 and NHIT/3. The time constant for the drift is a few minutes, though long periods of stability (hours) are also common. The drift is likely a temperature effect and if it proves to be a significant problem will have to be dealt with either by frequent threshold measurements or added hardware on the MTC/A.

In addition to the threshold variations, there is some distortion in the pulse shape coming from the CTC due to the long (60 foot) cables. The relatively slow discharge of the cables after a pulse input causes a small slope on the top of the pulse (5-10% from front to back), and the small mismatch in impedances of the cable and the MTC/A active termination

produces a reflection of $< 5\%$ of the pulse amplitude. While both these problems can be improved with the simple addition of a back termination, they result in a 50% loss of signal, making the MTC/A's inherent threshold drifts more serious. In the case of the reflection, the fix is of little value, since significant amplitudes occur only after large in-time coincidences which will trigger the detector and force a LOCKOUT as described in Section 8.

7.2 Digital Design

The three copies of the final analog sum are each referenced to +5 V through 50 Ohm resistors, and fed into one input of a fast, ECL comparator. This results in a typical DC offset voltage of roughly 4.7 V for each sum. The comparator operates within an input range of +5 V and -5 V, which gives nearly 10 V of dynamic range for the final analog sum voltages. For a nominal value of 30 mV/NHIT, this corresponds to an effective dynamic range from NHIT=1 to NHIT=320. For higher threshold settings, the 50 Ohm pullup resistor to +5 V can be made smaller, reducing the mV/NHIT slope. To avoid overvoltage at the comparator input, the final sum voltages are clamped with a diode which keeps them from falling below -5 V. With the 50 Ohm pullup, the dynamic range is roughly 300 tubes into the comparator. When the final analog sum voltage crosses a pre-programmed threshold voltage, the ECL output of the comparator is asserted (i.e. in a logical 'high' state) and will remain so until the threshold is crossed again by the trigger sum. This firing of the comparator signals a one shot to output a 20 ns ECL pulse which is sent to the MTC/D as the raw trigger pulse corresponding to the preset threshold.

The ECL one-shots on the MTC/A are operated non-retriggerably, which means, having once fired, they will not fire again until they receive a low-to-high transition on their input *after* the 20 ns pulse is completed. This means that even if a trigger sum is above threshold for a long period of time, the MTC/A would not retrigger. For this reason, additional logic exists on the MTC/A which samples the comparator output at the end of a full trigger cycle (see Sections 8 and Setion 2 for a discussion of LOCKOUT and the trigger cycle time) and retriggers if the comparator output is still asserted.

The MTC/A has three 12-bit serial DACs which provide individual threshold voltages to each of the comparators. The three trigger channels leading to raw triggers are identical except for the different DAC thresholds which can be programmed onto the comparator

inputs. These thresholds can be programmed between +5 V and -5 V in increments of 2.44 mV. The digital interface for the DAC programming is provided by the MTC/D (see Appendix H.3 for details). The DAC threshold voltages are also fed back to the MTC/D for monitoring purposes.

8 Master Trigger Card/Digital

The main role of the MTC/D in the SNO trigger system is to receive trigger pulses (whether physics triggers from the MTC/As, on-board generated calibration and monitoring triggers, or external triggers) and decide whether or not to trigger the detector by sending out a global trigger to the FECs. In addition, the MTC/D keeps time for SNO (both absolute GPS time and local inter-event time), counts and synchronizes the Event ID (global trigger number) for all the electronics, and stores all the relevant central event information (time stamps, event ID, trigger type, error flags, and measurements of the analog sum characteristics) in on-board memory for inclusion in the event header.

As shown in Figure 11, the main features are:

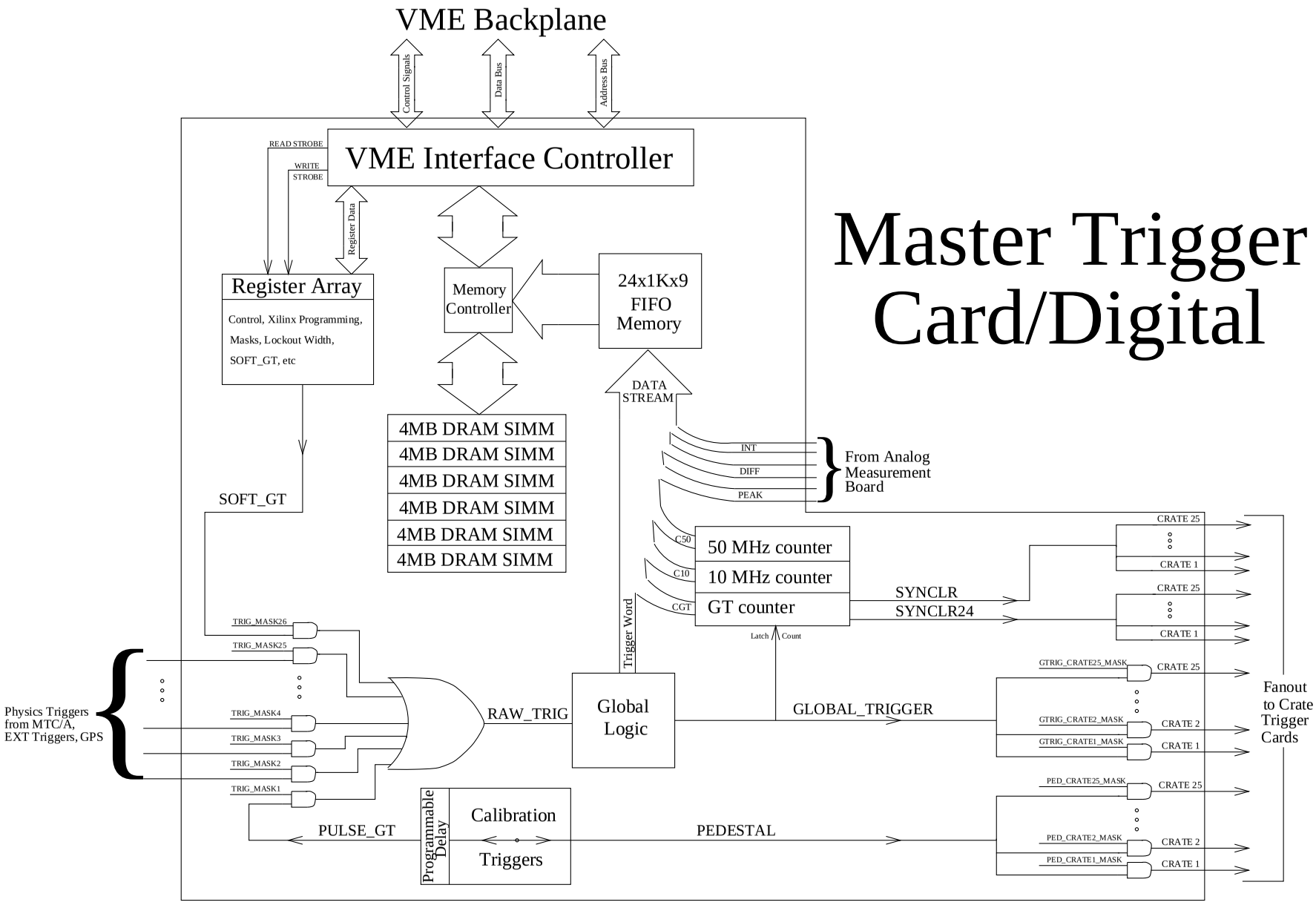
- *Global Trigger (GTRIG) generation*: Generation of global triggers synchronous to the master 50 MHz clock. Up to 26 different trigger types can lead to the generation of a global trigger, and the status of each trigger type is latched with each event and saved in a 'trigger word'.

- *Absolute time keeping*: Interface to GPS system to keep time with a resolution of 100 ns and an accuracy of $\sim$ 300 ns. GPS time is latched and saved with each event.

- *Inter-event time keeping*: Time between GTRIG's is kept by the synchronous master 50 MHz clock, whose count is latched and saved with each event.

- *Calibration/Monitoring triggers*: On-board generation of global triggers either as a fixed rate or through a software controlled pulser, as well as generation of timing ('Pedestal' or PED) signals with programmable delays relative to the GTRIG.

- *Fanout of timing signals*: Fanout of GTRIG, PED, and synchronous clear signals to all 20 crates plus five spares. The GTRIG and PED can be disabled for individual crates.



Master Trigger Card/Digital

Figure 11: Block diagram of Master Trigger Card/Digital.

- *Error and status flags*: Several error and status flags describing the state of the board (whether in testmode or data-taking mode, for example).

- *Fast memory*: Time counters, global trigger counter, trigger word, analog information, plus error flags are written to memory as six 4-byte longwords at rates that can exceed 4 MHz (96 MBytes/second) for times shorter than a few hundred milliseconds. Up to one million events can be stored on board, and the continuous data rate is limited only by the speed of readout by the DAQ.

- *Trigger thresholds*: Interface for programming NHIT and ESUM thresholds on MTC/A's, as well as measurement of the actual DC levels.

8.1 Global Trigger Generation

The global trigger is derived from candidate trigger pulses, each an ECL pulse roughly 20 ns long and each signifying that some potential trigger criterion has been satisfied. The candidates can originate on the MTC/A's due to a threshold crossing by the analog sum, by on-board pulsed trigger generation, or by external inputs to the MTC/D. Each candidate signal can be individually masked in or out (enabled or disabled) so that only certain types can initiate an MTC/D trigger cycle and generate a global trigger.

The 26 candidate trigger types are:

- *NHIT_100_LO*: Low threshold 100 ns trigger

- *NHIT_100_MED*: Medium threshold 100 ns trigger

- *NHIT_100_HI*: High threshold 100 ns trigger

- *NHIT_20*: Normal 20 ns trigger

- *NHIT_20_LB*: Look-back 20 ns trigger

- *ESUM_LO*: Low-gain energy sum trigger

- *ESUM_HI*: High-gain energy sum trigger

- *OWLN*: Outward looking tube 100 ns trigger

- *OWLE_LO*: Outward looking tube low-gain energy sum trigger
- *OWLE_HI*: Outward looking tube high-gain energy sum trigger
- *PULSE_GT*: Pulser generated calibration trigger
- *PRESCALE*: Prescaled NHIT_100_LO trigger
- *PEDESTAL*: Pedestal calibration trigger
- *PONG*: GPS round-trip delay trigger
- *SYNC*: GPS synchronization trigger
- *EXT_ASYNC*: External trigger not synchronized to 50 MHz clock
- *EXT8/PULSE_ASYNC*: External trigger/Asynchronous calibration trigger mask
- *EXT7..2*: External triggers
- *SPECIAL_RAW*: Logical combination of nine pre-selected triggers
- *NCD*: Neutral current detector trigger
- *SOFT_GT*: Software initiated trigger
- *MISS_TRIG*: Flag denoting that a masked in trigger arrived after the global trigger word had been latched

The rising edge of a masked-in candidate trigger pulse begins the trigger cycle, creating a 'raw' trigger pulse which is essentially an asynchronous global trigger. The raw trigger is synchronized to the 50 MHz clock creates the global trigger, and in addition generates a LOCKOUT pulse, which prevents any additional global triggers from being created for the duration of the trigger cycle. Because of the synchronization of the global trigger, the time between the firing of the raw trigger and the beginning of the global trigger depends upon the instantaneous phase of the 50 MHz clock, and will vary from 0 to 20 ns event to event. The beginning of the trigger cycle also leads to a delayed latch of all the bits in the trigger word, recording all the trigger types active at that same time as the one initiating the global trigger.

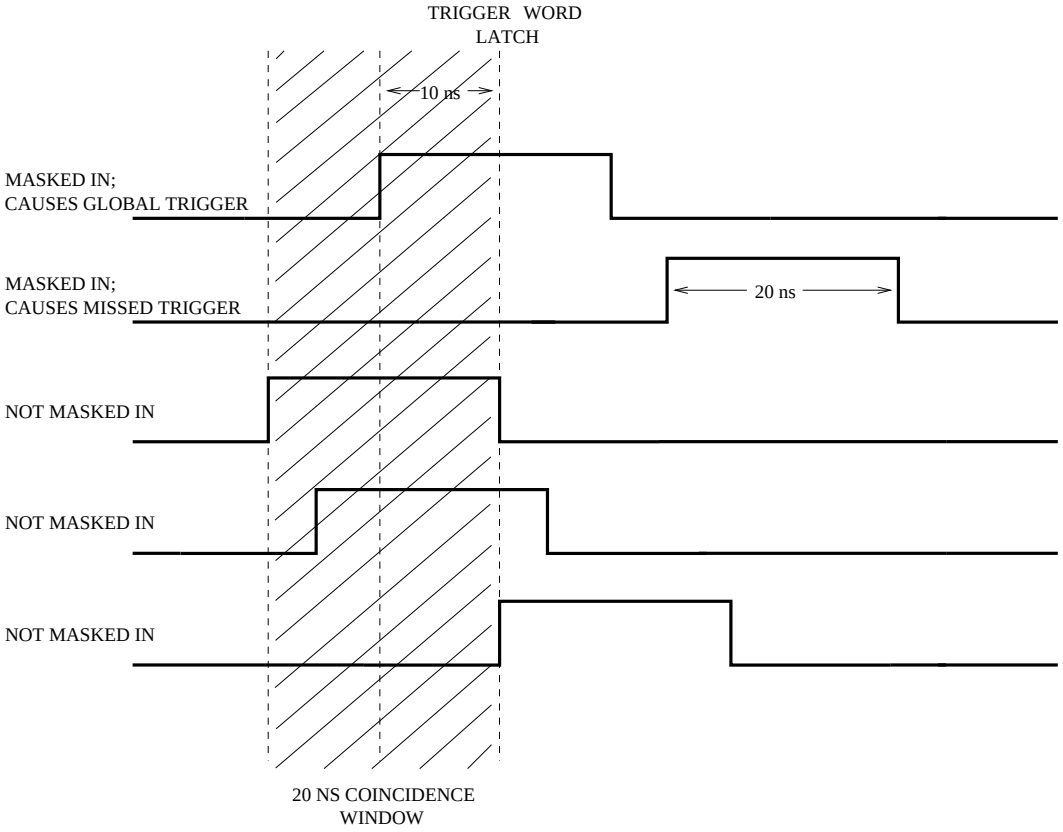


Figure 12: Diagram of coincidences between different trigger types and the latching of the trigger word.

The width of the global trigger pulse can be set to either 60 or 80 ns by jumpers on the board, and the LOCKOUT pulse width is programmable in 20 ns increments between 20 ns and 5μs. The delay of the trigger word latch, which determines how late a candidate trigger pulse can arrive and still be counted part of the trigger word, is nominally 10 ns but is adjustable through an RC circuit. With the nominal setting, all triggers within 20 ns coincidence of each other will be latched into the trigger word, assuming input candidate trigger widths of 20ns (see Figure 12). If any candidate trigger pulses arrive after this latch but before the end of LOCKOUT, an additional bit is set in the trigger word which flags it as a 'missed trigger'.

8.2 Trigger types

Of the trigger types listed above, a few require special comment. Unlike the other trigger types which are primitives representing a single trigger source, the SPECIAL_RAW trigger provides the capability of triggering on any logical combination of nine pre-selected triggers (see Appendix F for a list of these). The SPECIAL_RAW logic exists in one of the MTC/D Xilinx chips and can be reprogrammed 'on the fly' without bringing down the board. The SPECIAL_RAW trigger may be useful for cutting down the rate on low-energy background studies, or for look-ahead triggers where the trigger threshold is lowered for a specified window of time following a high-threshold trigger.

The EXT_ASYNC trigger is the only asynchronous trigger channel in which the global trigger generated from an external input is not synchronized to the 50 MHz clock. This is useful when the 20 ns raw trigger/global trigger jitter associated with synchronization is undesirable. In this case, LOCKOUT will be slightly longer than its programmed time, since it begins on the firing of the global trigger but counts clock cycles as if the trigger had been synchronous. So, for example, if LOCKOUT has been programmed to last 420 ns and the time between the raw trigger firing and the next tick of the 50 MHz clock is 12 ns, LOCKOUT will actually last 432 ns, since now the global trigger is as asynchronous as the raw trigger.

There is a prescaler on the MTC/D which will generate one PRESCALE candidate trigger pulse every time it receives a programmable number (SCALE) of NHIT_100_LO triggers. The MTC/D just prescales whatever signal is plugged into the NHIT_100_LO connector, so in actuality any trigger signal can be prescaled. The range of SCALE is from 2 to 65536 NHIT_100_LO triggers per PRESCALE. If the PRESCALE trigger is masked in it will generate a GTRIG and have its bit set in the trigger word. If, however, NHIT_100_LO is masked in, the MISS_TRIG rather than the PRESCALE bit will be set due to the timing of the PRESCALE trigger pulse relative to the trigger word latch.

8.3 Counters

The are three sets of counters on the MTC/D - the 50 MHz, 10 MHz, and global trigger counters. The purpose of the 50 MHz counter is to specify the relative time between events within the detector and is sourced from an external 100 MHz ECL oscillator. The counter

itself is 43 bits long, which means it rolls over once every 2 days. The 50 MHz count for an event is latched on the rising edge of global trigger. (See Appendix H.1 for a description of how the 50 MHz counter is loaded). The uncertainty in event-to-event times is roughly equal to the rms jitter in the edges of the 50 MHz clock, or less than a ns or so.

The 10 MHz counter provides a time of day stamp for an event within the detector using the Global Positioning Satellite (GPS) system. As shown in Figure 13, a GPS receiver on the surface communicates with the MTC/D through fiber-optic links and provides both the 10 MHz clock and synchronization (SYNC) pulse for loading the counter. This is a 53 bit counter providing times for up to 28 years without rolling over (although nearly two of those years will have ticked away by the time SNO begins since t_0 has been defined as midnight Jan 1, 1996) Loading of the counter is done only upon the arrival of a SYNC pulse from the GPS receiver, and the count loaded is pre-programmed by the DAQ system to agree with the time of the SYNC pulse generation (see SNO-STR "The Design of the SNO TIming System") for a detailed description of the timing procedure and Appendix H.1 for details on how the counter is loaded). The SYNC pulse also generates its own global trigger which latches and stores the 10 MHz count, so that the loaded time can be compared with what was intended. In order to correct for the delay between surface and lab, a 'PING' pulse is sent toward the surface on a separate fiber immediately after receipt of SYNC. After arrival of the PING at the surface, a pulse is immediately sent back down on the same fiber as the SYNC ('PONG'), generating another global trigger. Comparing the time of the SYNC global trigger (measured by the 50 MHz count) to the time of the PONG global trigger gives a measurement of the round trip fiber-optic delay with a resolution of 20 ns.

The 24 bit global trigger counter provides a unique event ID within a given run. Loading the global trigger counter is rather involved since the lower 16 bits and the upper 8 bits must be loaded independently (due to the independence of these bits on the Front End Cards), and since the loading must generate synchronous clear (SYNCLR) signals to both check and synchronize the global trigger counters on every channel of the electronics.

Each of the counters can be placed into a test mode to quickly verify that every element of the counter array is working properly. The way in which the counters operate in their respective test mode is different for each counter. In test mode, each byte of the 10 MHz counter will count independently. For the 50 MHz counter, each of the upper bytes will

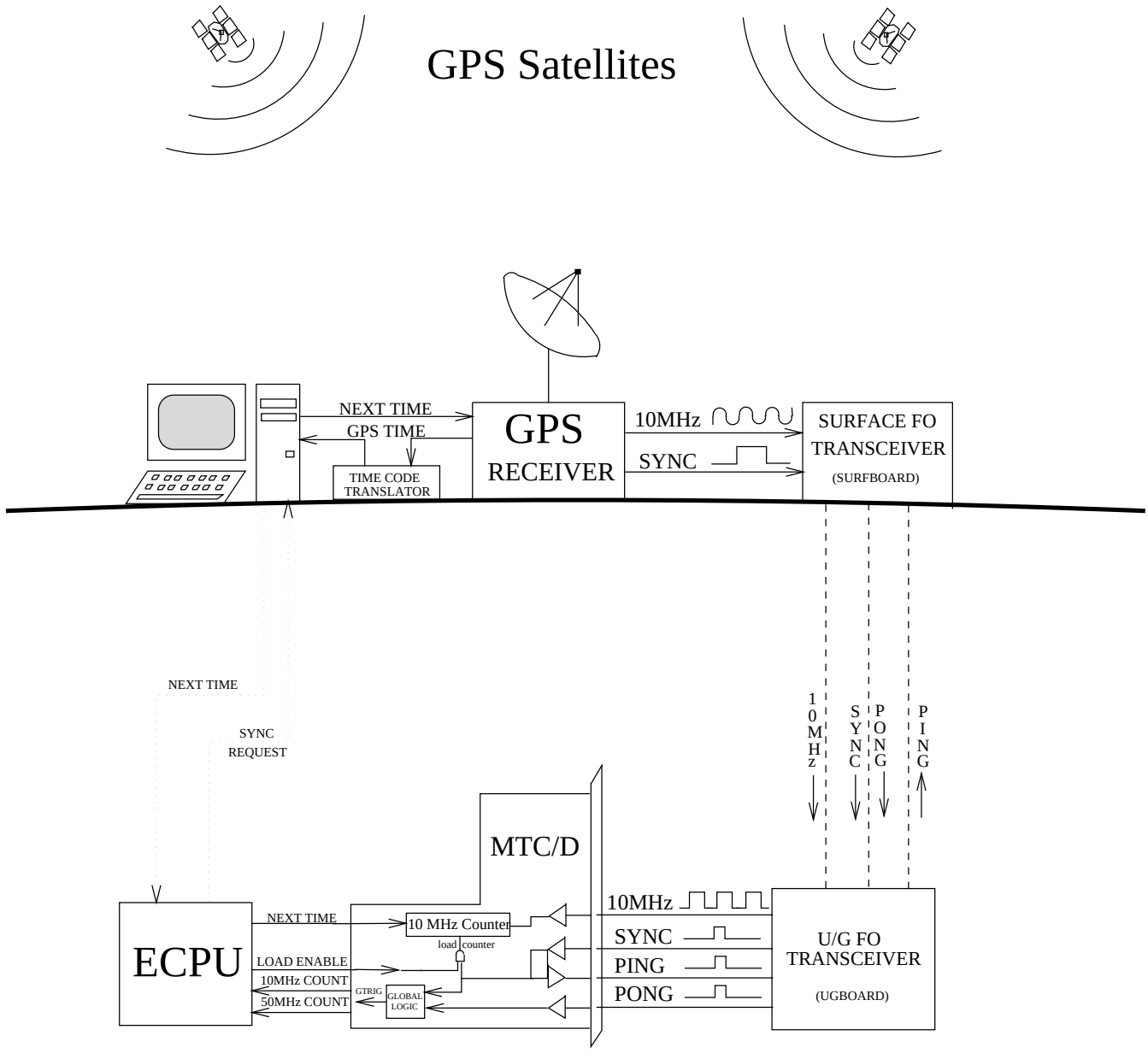


Figure 13: Block diagram of the GPS timing system.

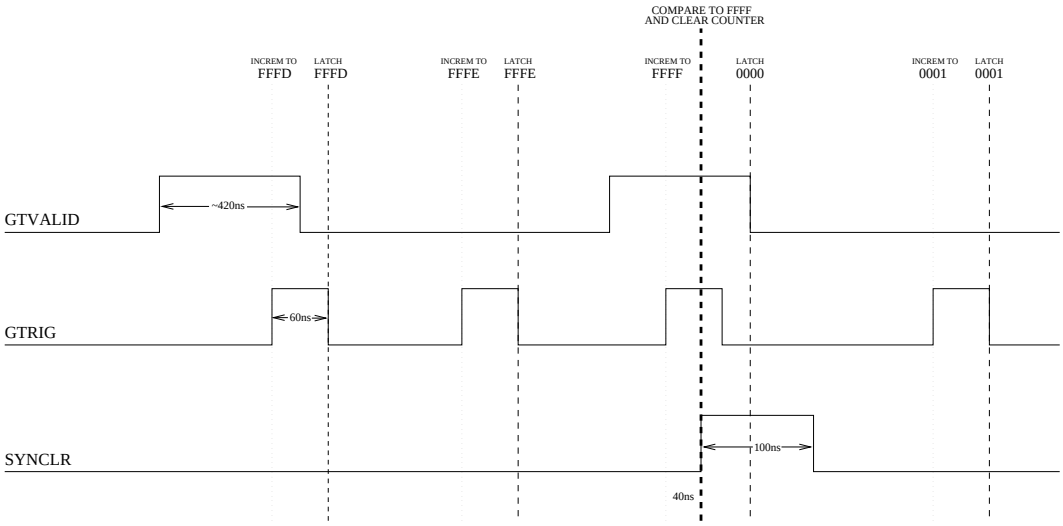


Figure 14: Timing and latching of GT ID with SYNCLR.

independently increment when the lower byte rolls over. The global trigger counter test mode is a combination of the above in that the lower two bytes count independently while incrementing the upper byte on their roll over (i.e. on SYNCLR).

There are two SYNCLR signals—SYNCLR and SYNCLR24, which clear the lower 16-bit counter on the CMOS chip and the upper 8 bit counter on the Motherboard, respectively. Under normal circumstances, a SYNCLR/SYNCLR24 pulse is sent out when the lower 16/upper 8 bits of the GT counter on the MTC/D roll over. The GT counter on the CMOS chip is incremented on the rising edge of GTRIG, but the count is latched into its digital storage array on the later of the falling edge of GTRIG and GTVALID. Therefore, the MTC/D must send out the SYNCLR pulses sometime during the GTRIG pulse to ensure that the count is always latched after SYNCLR clears the counter. Also, since the CMOS chip checks that its counter is at FFFF on SYNCLR before it is cleared rather than checking for 0000, numerous counts will never get latched into the storage array and become trigger IDs (see Figure 14). There are two other modes in which the MTC/D will generate SYNCLRs - RESYNC and ASYNC. In RESYNC mode, the MTC/D will send out both a SYNCLR and a SYNCLR24 when the lower 16 bits of the GT counter roll over. In ASYNC mode, SYNCLR and SYNCLR24 are sent out on every GTRIG without waiting for any counter roll over. Both of these latter modes can be used when a new run—defined as

beginning with a GTRIG count of 0000— is initiated by a user.

8.4 Channel Timing and Other Calibrations

The MTC/D has the responsibility of generating pulses for calibration of Front End channel timing and charge. These pulses are referred to as 'Pedestal' or just 'PED' pulses because one of their uses is to measure the ADC charge pedestal by firing the SNO discriminators in the absence of charge, are used to fire charge injection circuitry on the PMT Interface Cards for channel charge tests and to provide measurements of channel timing (TAC timing) by arriving at programmed times relative to an accompanying pulsed global trigger.

The pulsed global trigger is produced from an internal trigger signal (PULSE_GT) and can be either asynchronous or synchronous to the 100 MHz clock, depending on the bit set in the trigger mask. The PED and PULSE_GT pulses can be generated in a number of ways. The first and simplest way is to use the on-board pulser which can generate PED and global trigger pulses at a programmable rate between 390 kHz and 0.04 Hz. On the other hand, if a precise number of PED events is desired, the MTC/D can use software initiated pulses (SOFT_GTs) in place of the pulser. However, one must be careful when using SOFT_GT's for calibrations of timing. A bug in the synchronization hardware allows about 5% of the global triggers accompanying a SOFT_GT-initiated PED pulse to appear 20 ns early. Therefore an offline cut must be placed around the main peak in order to get the correct mean and rms for the measured PED-GTRIG delay when using SOFT_GT's. If one wants ultimate flexibility in PED generation, the MTC/D also has an external pedestal input (EXT_PED) where pedestal events can be generated by a external source such as a pulser.

Some control over the pulse width and relative delay of pedestal event pulses is required for charge injection and TAC slope measurements. In the case of charge injection, the total amount of charge injected by the PMT Interface Card is proportional to the PED width. This width is programmable in 5 ns increments from 5 ns to 1.275 μs. The relative delay between PED and the internal trigger signal PULSE_GT can be varied using a coarse 10 ns delay relying on the 100 MHz clock and a fine delay (100 ps increments) coming from a programmable delay chip. If the GTRIG is generated asynchronously, then it will have the full 100 ps delay resolution of the PULSE_GT pulses. However, if the GTRIG is generated

synchronously, it can only be delayed in 20 ns increments but will be synchronous to the 100 MHz clock. The relative delay is programmable between 24 ns and 2574 ns, with the 24 ns offset resulting from gate and trace delays inherent to the board. Both PED and GTRIG can be independently delayed with cables that plug directly into the front panel, so any desired offset can be attained. The MTC/D can also be used to generate double PED pulses by feeding the GTRIG output of a spare fanout connector back into the EXT_PED input. The relative delay between the two PED pulses is then controlled by varying the coarse and fine delay settings as in the PED/GTRIG delay.

8.5 Memory

The memory front end consists of 24 1Kx9 FIFOs which act to buffer the incoming 192 bits of data before going to the memory modules. All of the FIFOs are written to in parallel on the trailing edge of LOCKOUT, which signifies the end of an MTC/D trigger cycle. The FIFOs then remove their empty flags, signaling to the memory controller that they have data. At this time the controller will attempt to move the data from the FIFOs to the DRAM SIMMs as long as the FIFOs still have data and the memory controller is not currently servicing a VME read request. There are six 32-bit 4MB SIMMs which are written to in parallel at a maximum rate inversely related to the LOCKOUT width. For a nominal LOCKOUT width of 400 ns, this corresponds to a rate of 60 MB/sec.

The memory is read out through the VME in a two step process. The memory location to be read from is first written to the Buffered Board Address (BBA) register. It is important that the memory addresses written to this register be sequential for proper handling of the read/write pointers by the memory controller. It is for this reason that the address is passed through this register rather than taken from the VME address bus, so the DAQ can directly access where it read from last. After writing the memory address to the BBA register, the VME then generates six memory read requests, one for each SIMM on the MTC/D. The memory controller will then cycle through each of the six SIMMs, placing one 32-bit long word per SIMM on the data bus for the VME controller to latch.

There are two special memory modes which allow more direct access to the memory through VME - TESTMODE1 and TESTMODE2. In TESTMODE2, all six SIMMs can have the same value written to them through VME to the memory location stored in the

BBA register. Memory reads in TESTMODE2 are identical to normal mode memory reads. TESTMODE1 differs from TESTMODE2 in that any individual SIMM can be written to or read from through VME. The desired SIMM is specified through the three highest BBA register bits. The two memory testmodes are entered by setting appropriate bits in the control register. TESTMODE2 is enabled by setting the TESTMEM2 bit and TESTMODE1 is entered by setting both TESTMEM1 and TESTMEM2 bits.

8.6 Fanout

The MTC/D handles the fanout of four ECL signals to the Crate Trigger Cards - PED, GTRIG, SYNCLR, and SYNCLR24. There are 25 fanout connectors through which these four signals are driven - 20 crate connectors and five spares. While SYNCLR and SYNCLR24 are always sent to each fanout connector, the PED and GTRIG pulses can be sent through any combination of fanout connectors. This selective fanout of PED and GTRIG is specified by setting the appropriate crate mask bit(s) in the pedestal crate mask (PMSK) and global trigger crate mask (GMSK) registers, respectively.

8.7 Trigger Thresholds

The MTC/D provides the digital interface for the programming and monitoring of the MTC/A threshold DACs. The MTC/A DACs require three control signals for programming - serial data, a clock, and a select, which are driven by a register on the MTC/D (DAC_CNT). The register contains separate serial data lines for each MTC/A DAC threshold, but just a single clock and select lines which go to each DAC. Therefore, while a given DAC is programmed serially, all the DACs on the MTC/A are programmed in parallel.

The MTC/A DAC thresholds are connected directly to the MTC/D for monitoring purposes. A 16:1 analog multiplexer is used to select which of the ten thresholds are driven onto the input of a continuously converting 12-bit ADC for digitization. The threshold which gets selected (multiplexed) is determined by a set of five control register bits labeled TMON0..3 and TMONSEL. A snapshot of the ADC outputs is taken when a VME read is performed on a register called THRESHMON. This is a 13-bit register which displays not only the 12-bit ADC value but also a BUSY bit that flags a conversion was in process when the ADC output was latched.

8.8 Error and Status Flags

There are several error and status flags set in the MTC/D datastream which are used to describe the state of the board at the time of an event. These flags are included in the event header and are summarized below:

- *Counter test modes*: 50 MHz, 10 MHz, and global trigger counter testmode status flags.
- *Memory test modes*: TESTMEM1 and TESTMEM2 memory testmode status flags.
- *Synclr conditions*: Flags which indicate that SYNCLR and/or SYNCLR24 occurred and whether or not they were the result of RESYNC or ASYNC mode.
- *FIFO error conditions*: Error flags which are set when FIFOs have different empty/full status or are full.

A bit-by-bit description of the flags can be found in Appendix B.

9 Auxiliary Trigger Boards

There are four special-purpose boards in the trigger system. These boards are not all manufactured as printed circuit boards because of their low quantity (1/system) and their relative simplicity.

9.1 Analog Crate Interface Card

The crate which holds the MTC/A's also contains a simple board which interfaces to the MTC/D. This board transmits the DAC programming lines as well as the threshold outputs of each of the MTC/A's monitored by the MTC/D. Because the multiplexer on the MTC/D used to switch between the threshold lines cannot have a negative voltage on any of its inputs, the thresholds from the MTC/A need some special handling. Since it is unlikely that the thresholds for most of the trigger lines will ever be set negative for a significant amount of time (negative voltage means high threshold—$\sim$ NHIT of 160 for the NHIT100 lines—see Section 7.2), the threshold lines are simply clamped with Schottky diodes to ground. This

means that although the thresholds can be set negative, the MTC/D will not be able to correctly monitor them during that time.

The exception is the is the NHIT_100_HI line, since it is the most likely to be set at a high threshold that will need to be monitored. For this line, a simple op-amp absolute value circuit is used, with the assumption that the user will know the sign of the threshold that has been programmed.

These DAC threshold settings are not only sent to the MTC/D for digitization, but are also sent to a socket on the Analog Crate Interface Card front panel for more direct measurement with a voltmeter. The threshold to socket pin mapping is presented in Appendix G.

The Analog Crate Interface Card also provides the connection between the MTC/D and the serial register array on the Trigger Utility Board which is primarily used for controlling the PSUP LEDs. This is described in more detail in Section 9.3.

9.2 Fiber Optics Drivers and Receivers

As described in Section8.3, the signals from the GPS receiver are carried on fiber optic cables to the MTC/D. In addition, the MTC/D sends a pulse up one of the fibers to the surface as a measurement of the delay along the fibers. Two small boards, one on the surface (Surfboard) and one underground (UGboard), handle the transmitting and receiving of the optical pulses.

The Surfboard receives the electronic 10 MHz and SYNC signals from the GPS receiver and transmits them to the UGBoard as light pulses along fiber optic links. It also receives a PING light pulse (initiated by a SYNC on the MTC/D) from the UGBoard and re-transmits it as a PONG light pulse to the UGBoard for a determination of the round trip fiber optic delay.

The UGBoard provides the fiber optic interfacing to MTC/D. It receives the optical 10 MHz and SYNC pulses from the Surfboard and sends these to the MTC/D as single-ended ECL signals. The UGBoard also transmits the PING pulse from the MTC/D to the Surfboard and recieves the reflected optical PONG signal to send back to the MTC/D.

9.3 Trigger Utility Board

The Trigger Untility Board (TUB) holds many special-purpose circuits that proved useful during the debugging and designing of the trigger system, as well as some features necessary for the operation of the full system. The board will be mounted in the rack near the MTC/D, and has several utilities:

- *100 MHz Clock*: Source and driver of 100 MHz ECL clock for MTC/D. Clock indicator LED.
- *Fanout of LOCKOUT*: Fanout of LOCKOUT signal from MTC/D to the seven MTC/A boards for retriggering. TTL LOCKOUT spare.
- *Timebus Translation*: Translation of differential ECL timebus signals GTRIG, PED, SYNCLR, and SYNCLR24 on 10-pin connector to TTL BNC connectors.
- *Discriminator with Retriggering*: Essentially an MTC/A without analog summing. Threshold discrimination of a positive or negative-going analog pulse to produce a 20ns ECL trigger pulse. Retriggering on LOCKOUT option set with jumper.
- *TTL Pulse LED Indicator*: General-purpose indicator which lights an LED on the rising edge of an input TTL pulse.
- *TTL⇔ECL Translations*: Several TTL→ECL and ECL→TTL translation ports.
- *BNC⇔SMB Conversions*: Several BNC⇔SMB connector conversion ports.
- *TIMEBUS Speaker*: Listen to pulses from your favorite TIMEBUS channel - PED, GTRIG, SYNCLR, or SYNCLR24.
- *Serial Register Array*: Primarily for controlling the PSUP LEDs, this is a 32-bit register which is serially programmed from spare bits in the DAC programming register on the MTC/D. The outputs corresponding to the serially programmed data become valid on the rising edge of the serial latch.

9.4 Analog Measurement Board

In order to save some information about the analog sum itself, the trigger system includes a board which measures and digitizes characteristics about the analog sum. Specfically, the Analog Measurement Board (AMB) measures the peak, the derivative as threshold is crossed, and the integral of the analog sum each time a Global Trigger occurs. Only one of the analog sums can be input to the AMB at a time. Nominally the NHIT_100 sum will be conected, as this is intended to be the main analysis trigger.

The analog part of the measurements are simple op-amp circuits, with RESETs for the peak detector and integrator made from differential pairs driving fast JFETs. The digitization is done by 8-bit flash ADC's and driven off the AMB and on to the MTC/D, where it is written into memory with each event.

The derivative is taken just as the analog sum crosses threshold, and provides information about how in-time the tubes are that are contributing to the sum. Cases where the threshold is crossed by a straggler tube will have much smaller derivatives than cases where many in-time tubes are summed together.

Both the integral and the peak are applied to slightly delayed copies of the analog sum. The integral measures all the charge in the analog sum from about 20 ns before the threshold crossing to 60 ns after, and provides information about the shape of the sum. The peak is also measured until roughly 60 ns after the threshold crossing, and allows a simple check on whether the height of the analog sum agrees with the offline reconstructed total NHIT.

A CMOS Shift Register Bits

As described in R. L. Stevenson's *Chip Description Document* for the SNO CMOS chip (QUSN7), the CMOS shift register holds 35 bits, 17 for the trigger pulse widths and delays and 18 for other CMOS functions. The data is shifted in high bit first. We reproduce here the bit mapping for the trigger controls, with the progammed widths delays as measured in the real system. The minimum width for the NHIT100 pulses is roughly 10 ns; for NHIT20 it is 7 ns. The measured values all have uncertainties of ± 1.5 ns.

Table 1: Bit Mapping for CMOS Shift Register Trigger widths and Delays

Trigger Signal	Bit	Function
NHIT100	0	Adds 1.5 ns to width
	1	Adds 2.5 ns to width
	2	Adds 5.0 ns to width
	3	Adds 10.0 ns to width
	4	Adds 20.0 ns to width
	5	Adds 40.0 ns to width
	6	Mask (Enable) Bit
NHIT20	7	Adds 1.5 ns to delay
	8	Adds 2.5 ns to delay
	9	Adds 5.0 ns to delay
	10	Adds 10.0 ns to delay
	11	Adds 1.5 ns to width
	12	Adds 2.0 ns to width
	13	Adds 4.0 ns to width
	14	Adds 10.0 ns to width
	15	Adds 20.0 ns to width
	16	Mask (Enable) Bit

B MTC/D Memory Bit Mapping

The following table describes the mapping and definitions of all the bits in the MTC/D memory. Figure B illustrates the same information diagrammatically.

Table 2:

SIMM(s)	Bit(s)	Description
0,1	0..31,0..20	10 MHz count (53 bits)
1,2	21..31,0..31	50 MHz count (43 bits)
3	0..23	Global Trigger count (24 bits)
3,4	24..31,0..17	Trigger Word (26 bits)
4	18	Missed Trigger occurred
4	19..28	Digitized voltage peak after crossing threshold
4,5	29..31,0..6	Digitized voltage slope after crossing threshold
5	7..16	Digitized integral near threshold crossing
5	17	0 if in GT counter testmode
5	18	0 if in 50MHz counter testmode
5	19	0 if in 10MHz counter testmode
5	20	Status of testmem1 bit in control register
5	21	Status of testmem2 bit in control register
5	22	SYNCLR was generated
5	23	SYNCLR was generated w/o 16-bit rollover of GT counter
5	24	SYNCLR24 was generated
5	25	SYNCLR24 was generated w/o 24-bit rollover of GT counter
5	26	FIFOs do not all have the same empty status
5	27	FIFOs do not all have the same full status
5	28	FIFOs are full
5	29..31	Not used

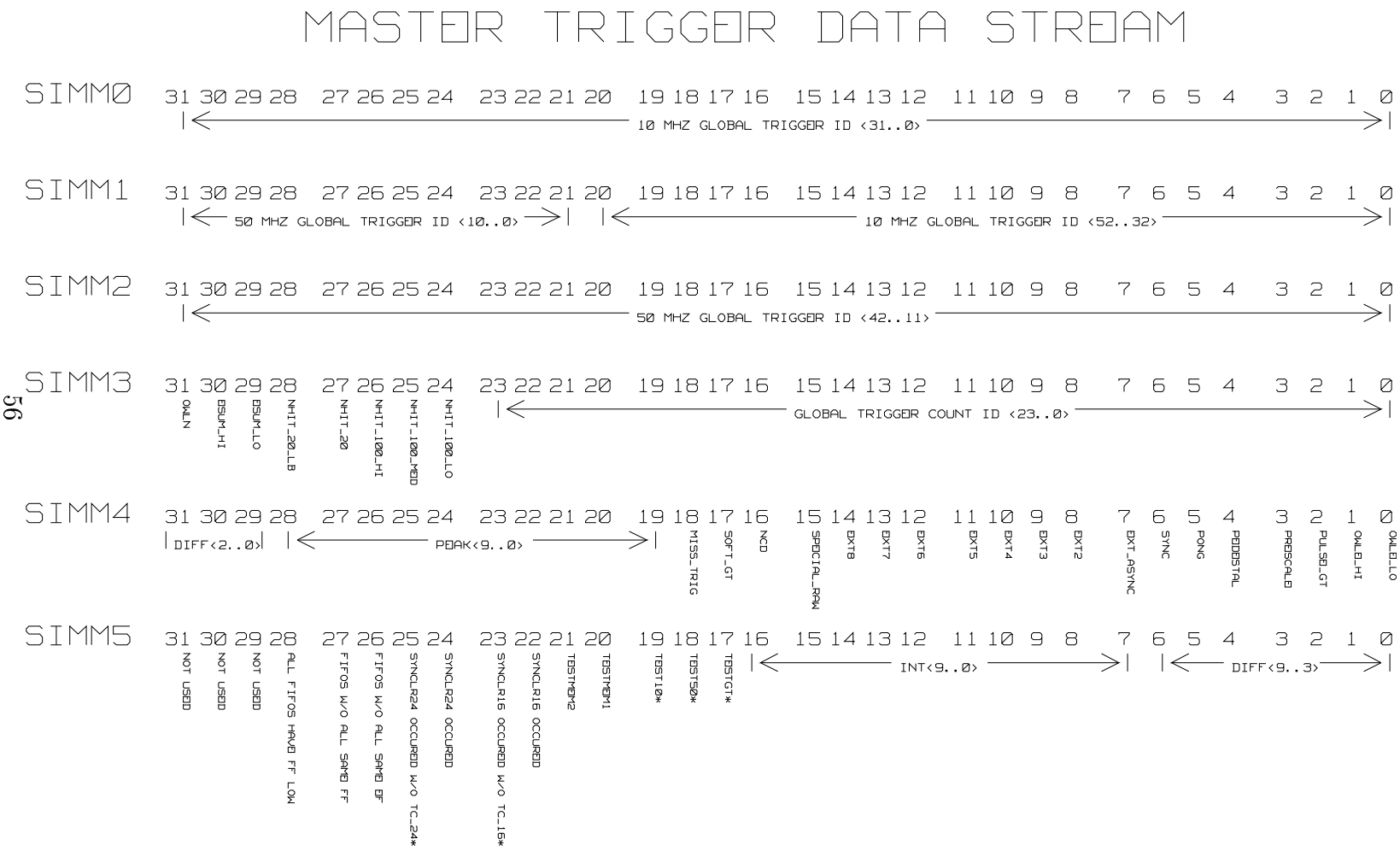


Figure 15: Representation of bits in MTC/D memory.

C Mapping of CTC Register Bits to NHIT20 Delays

The single register on the Crate Trigger Card (at address 0x90) controls the delays of the 20 ns trigger signals for each FEC as described in Section 6.2. The register is 32 bits wide, and two bits are allocated to each FEC, beginning with bits 0 and 1 corresponding to FEC 0, bits 2 and 3 for FEC 1, etc. The following truth table describes how each pair of bits is mapped to the off-board delays of the CTC:

Table 3: Truth Table for Bits Used for NHIT20 Delays on CTC

High Order Bit	Low Order Bit	Delay
0	0	0 ns
1	0	20 ns
0	1	40 ns
1	1	60 ns

D Backplane Jumper Configuration

The way in which the SNO Backplanes handle the trigger signals from the 16th Motherboard slot depends on whether it is configured normally or as an Outward-looking (OWL) Backplane. The particular Backplane configuration depends on which of the following jumper sets are in place:

Normal Configuration				OWL Configuration			
Connect	TP15	to	TP16	Connect	TP17	to	TP20
	TP18		TP30		TP19		TP26
	TP23		TP25		TP21		TP28
	TP28		TP31		TP27		TP30
	TP33		TP40		TP29		TP32
	TP34		TP39		TP33		TP41
	TP35		TP38		TP34		TP42
	TP36		TP37		TP35		TP43
	TP45		TP46		TP36		TP44

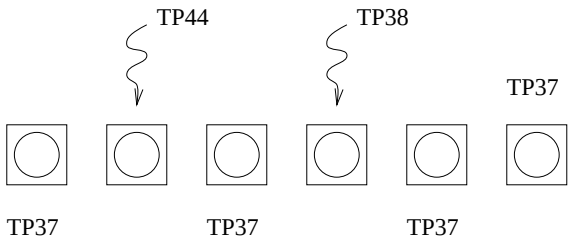


Figure 16: Diagram of labelling of backplane testpoints.

E Setting and Tuning Bias Currents on the CTC

E.1 Crate Bias Current Mirror

As described in Sections 4 and 6.1, the bias current for both NHIT100 and NHI20 trigger circuitry on the Daughterboards is supplied by two (nearly identical) current mirrors on the Crate Trigger Card (CTC). The current mirror acts as a voltage compliant, constant source of current for the Daughterboards as well as a source for subtracting off excess bias when the signals reach the CTC. Figure 17 illustrates one of the mirror diagrammatically.

The current sourced and sunk from these mirrors can be 'tuned' in two different places, labelled in Figure 17 as R_p and R_E. R_p are four parallel resistors which set the bias level for the entire crate. One end of these resistors is tied to +24 V, the other to the input of the 'programming stage' for the current mirror. The current mirror's bottom reference is -24 V, but the input to the mirror sits at about -21 V due to V_{BE} drops in the transistors, producing a voltage drop across the resistors at R_p of about 45 V. The 45 V/R_p of current input into the progamming stage is multiplied by four before being sent out to the Daughterboards (in reality, sunk from them) as bias. For example, if a bias current of 1.5 mA/DB is desired, the total current in the crate needs to be about

$$1.5\text{mA} \times 64 = 96\text{mA}.$$

The current into the programming stage is 1/4 of this, and so the resistance at R_p must be

$$R_p = 45\text{V}/24\text{mA} = 1875\Omega.$$

Four parallel resistors are used to dissipate the power, which corresponds to each resistor having a value of 7500Ω.

The second tuning point (R_E) is somewhat more subtle. As shown in Figure 17 and discussed in Section 6.1, the first current subtraction (F) is done using an inverted copy of the programming current (I), multiplied by a gain of 3 (or 3/4 of the total bias current sunk from the DB's). The inversion is required for a subtraction of current rather than an addition. The inverting current mirror is programmed with a copy (C) of the current biasing the DB's. However, if the voltage seen by the stage biasing the DB's (B) is different than the voltage seen by the stage programming the inverting current mirror, then the Early effect

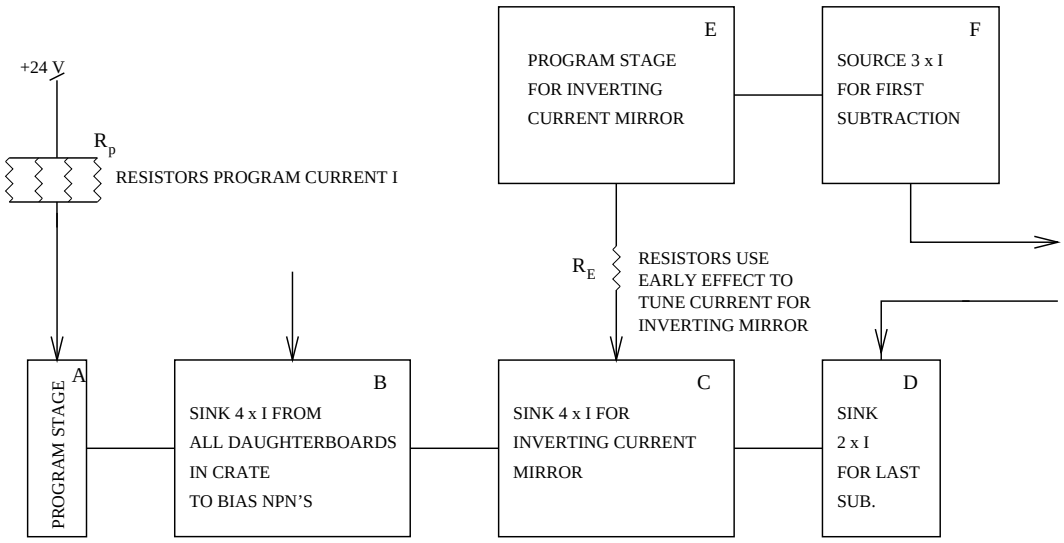


Figure 17: Block diagram of one of the ESUM trigger sums.

will lead to different currents in the two. The resistors at R_E act to ensure that the voltage seen by C is the same as that seen by B. This voltage can be calculated from a knowledge of the base references of the common-base NPN summing nodes on the DB and the total bias current. With 3.3 V at each base (see Section 4), the voltage at the emitter of each of the summing nodes is $\sim$2.5 V. The series resistance between the bias current source and each emitter is $\sim$ 7kΩ, so all 64 in a crate yield a parallel resistance between the current mirror and 2.5 V of $\sim$ 110Ω. The voltage seen by B is therefore

$$2.5\text{V} - (96\text{mA} \times 110\Omega) = -8.1\text{V}.$$

The voltage at the input to E is roughly 21 V, and therefore for C to see the same voltage as B, we must have

$$R_E = (21\text{V} - (-8.1\text{V}))/96\text{mA} = 303\Omega.$$

In practice the resistance that tunes this voltage is made up of a combination of 10 parallel and series resistors to minimize the power dissipation of any one resistor.

The stage labelled D in Figure 17 is the current subtracted from the output of the CTC before the signal is sent to the MTC/A. This subtraction does not need to be inverted, since before the output the signal itself is inverted. Although the first subtraction by F is 3/4 of the current sent to the DB's by B, we must subtract off 1/2 of this total at the output

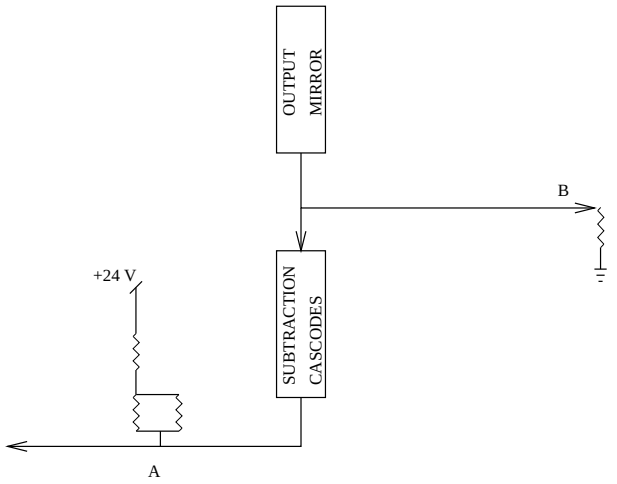


Figure 18: Diagram of final tuning resistors.

because the final stage in the CTC current sum has a gain of 2.

E.2 Output Tuning

As indicated by the previous section, the fact that the bias and the subtraction current come from the same mirror means that in principle the net current left at the output is zero. However, in practice this is not true because the path taken by the original bias current (through the DB's, the CTC active terminations, summing nodes, and output current mirror) has more losses due to the finite β of the transistors than does the current used for subtraction. Left alone, therefore, the DC offset at the output of the CTC (taken across a 50 Ohm resistor load, for example) would be somewhat negative. Measurements of the mismatch between the current sourced to the DB's and the current subtracted show it to be roughly 6 mA.

To correct the problem, a combination of three large resistors is used to reduce the subtraction current, as shown in Figure 18. The voltage looking in to the subtraction cascodes (the voltage at A) is $\sim -6V$. In order to eliminate the extra 6 mA of subtaction current coming from the biassing current mirror, the resistance of the combination of the three resistors labell R_T must be

$$(24\text{V} - (6\text{V}))/6\text{mA} = 5\text{k}\Omega.$$

To correct for different offsets for individual CTCs, these resistor values can be varied slightly.

F SPECIAL_RAW Trigger

The SPECIAL_RAW trigger provides the capability of triggering on any logical combination of nine pre-selected triggers, which are shown below:

1 **NHIT_100_LO**

2 **NHIT_100_MED**

3 **NHIT_20**

4 **ESUM_LO**

5 **ESUM_HI**

6 **OWLN**

7 **OWLE_LO**

8 **NCD**

9 **EXT5**

G Analog Crate Interface Card Threshold Socket

The DAC threshold settings are sent to a socket on the Analog Crate Interface Card front panel for more direct measurement with a voltmeter. The threshold to socket pin mapping (with all other pins at ground) is shown in Table 4:

Table 4: Threshold Socket Pinout

Pin	Threshold
1	OWLE_HI
8	NHIT_20_LB
9	NHIT_100_HI
10	ESUM_HI
11	NHIT_100_MED
12	OWLN
13	NHIT_100_LO
14	ESUM_LO
15	NHIT_20
16	OWLE_LO

H MTC/D Register List

Table 5: MTC/D Register Description

Register	No. of Bits	Title	Description	Read/Write
0	32	CONTROL	Enables for testmodes, loadling counters, etc	R/W
1	8	SERIAL	Serial data and clocks for counters, pulser	R/W
2	16	DAC_CNT	MTC/A Threshold DAC programming lines	R/W
3	-	SOFT_GT	Software generated raw trigger	W
4	8	PWID	Pedestal width	R/W
5	8	RTDEL	Coarse 10ns PED→ PULSE_GT delay	R/W
6	8	ADDEL	Fine <100ps PED→ PULSE_GT delay	R/W
7	13	THRESHMON	MTC/A Thresholds readback	R
8	25	PMSK	Pedestal fanout mask	R/W
9	16	SCALE	Scale for prescaling of NHIT_100_LO	R/W
10	20	BWR_ADD_OUT	Next memory write pointer	R
11	23	BBA	Memory read pointer	R/W
12	8	GT_LOCK	LOCKOUT width	R/W
13	26	MASK	Global trigger mask	R/W
14	8	XILPROG	Xilinx programming control	R/W
15	25	GMSK	Global trigger fanout mask	R/W
16	24	OCGT	Global trigger count	R
17	32	C50_LOWER	50 MHz counter (bits 0..31)	R
18	11	C50_UPPER	50 MHZ counter (bits 42..32)	R
19	32	C10_LOWER	10 MHZ counter (bits 42..31)	R
20	21	C10_UPPER	10 Mhz counter (bits 52..32)	R

Detailed register discription:

H.1 CONTROL Register

- *Bit0 PED_EN* - Enable for pedestal pulse generation.
- *Bit1 PULSE_EN* - Enable on-board pulser for pedestals, PULSE_GTs.

- *Bit2 LOAD_ENPR* - Prescale load enable. Toggling this bit loads the SCALE value into the prescaler.
- *Bit3 LOAD_ENPS* - Pulser load enable. Toggling this bit loads the programmed period into the pulser.
- *Bit4 LOAD_ENPW* - Pedestal width load enable. Toggling this bit loads the pedestal width (PWID) and the coarse PULSE_GT delay (RTDEL) into the ped/delay generator.
- *Bit5 LOAD_ENLK* - Lockout load enable. Toggling this bit loads the LOCKOUT width (GT_LOCK) into the LOCKOUT pulse generator.
- *Bit6 ASYNC_EN* - AYSNC mode enable. In ASYNC mode, the MTC/D will generate both SYNCLR and SYNCLR24 on a global trigger. After the first GTRIG, ASYNC mode is automatically disabled.
- *Bit7 RESYNC_EN* - RESYNC mode enable. In RESYNC mode, the MTC/D will generate both SYNCLR and SYNCLR24 on each GT counter 16-bit rollover.
- *Bit8 TESTGT* - GT counter testmode enable. See Section 8.3 for details.
- *Bit9 TEST50* - 50 MHz counter testmode enable. See Section 8.3 for details.
- *Bit10 TEST10* - 10 MHz counter testmode enable. See Section 8.3 for details.
- *Bit11 LOAD_ENGT* GT counter load enable. Toggling this bit generates a SYNCLR and a SYNCLR24 which load the programmed count into the lower 16-bits and the upper 8 bits of the GT counter, respectively.
- *Bit12 LOAD_EN50* - 50 Mhz counter load enable. Toggling this bit loads the programmed count into the 50 MHz counter.
- *Bit13 LOAD_EN10* - load enable. After toggling this bit, the programmed count will get loaded into the 10 MHz counter on the next SYNC pulse from the GPS.

- *Bit14 TESTMEM1* - Memory testmode bit 1. When set, allows any individual SIMM to be written to or read from through VME. The SIMM is selected by the three highest bits in the BBA register. See Section 8.5.

- *Bit15 TESTMEM2* - Memory testmode bit 2 . When set, allows all six SIMMs to have the same value written to them through VME. See Section 8.5.

- *Bit16 FIFO RESET* - When set, all FIFO pointers internal to the memory controller are reset to zero.

- *Bits17..21* Threshold monitoring control. Bits 17..20 specify which MTC/A DAC threshold to monitor as shown in Table 6.

Table 6: Threshold Monitoring Control

Threshold	Bit20	Bit19	Bit18	Bit17
NHIT_100_LO	0	0	0	1
NHIT_100_MED	0	0	0	0
NHIT_100_HI	0	0	1	1
NHIT_20_LB	0	0	1	0
NHIT_20	0	1	0	1
ESUM_LO	0	1	0	0
ESUM_HI	0	1	1	1
OWLE_LO	1	0	0	1
OWLE_HI	1	0	0	0
OWLN	0	1	1	0

Bit21 is an disable of the multiplexer which drives the selected threshold voltage to the input of the ADC for digitization (0=enable, 1=disable).

H.2 SERIAL Register

- *Bit0 SEN* - Enables serial loading of all shift registers on board.

- *Bit1 SERDAT* - Serial data which goes to all shift registers on board.

- *Bit2 SHFTCLKGT* - GT counter shift clock. One bit of serial data is loaded into GT counter shift registers on the rising edge of the clock. This value then gets loaded into the counter using LOAD_ENGT.

- *Bit3 SHFTCLK50* - 50 MHz counter shift clock. One bit of serial data is loaded into 50 MHz counter shift registers on the rising edge of the clock. This value then gets loaded into the counter using LOAD_EN50.

- *Bit4 SHFTCLK10* - 10 MHz counter shift clock. One bit of serial data is loaded into 10 MHz counter shift registers on the rising edge of the clock. This value then gets loaded into the counter on SYNC using LOAD_EN10.

- *Bit5 SHFTCLKPS* - Pulser shift clock. One bit of serial data is loaded into pulser shift registers on the rising edge of the clock. This value (SP) then gets loaded into the pulser using LOAD_ENPS. The pulser period is then $(\mathrm{SP}+1)\times 1280$ ns for $\mathrm{SP}\neq 0$. When $\mathrm{SP}=0$, SOFT_GTs are used as the source for the pulser rather than the clock.

H.3 DAC_CNT Register

- *Bit0 DACDAT0* - NHIT_100_LO serial data

- *Bit1 DACDAT1* - NHIT_100_MED serial data

- *Bit2 DACDAT2* - NHIT_100_HI serial data

- *Bit3 DACDAT3* - NHIT_20 serial data

- *Bit4 DACDAT4* - NHIT_20_LB serial data

- *Bit5 DACDAT5* - ESUM_HI serial data

- *Bit6 DACDAT6* - ESUM_LO serial data

- *Bit7 DACDAT7* - OWLE_HI serial data

- *Bit8 DACDAT8* - OWLE_LO serial data

- *Bit9 DACDAT9* - OWLN serial data

- *Bit10 TUB_SDATA* - Serial data for TUB serial register array
- *Bit11 TUB_SCLK* - Serial clock for TUB serial register array
- *Bit12 TUB_SLATCH* - Serial latch for TUB serial register array
- *Bit13 DACDAT13* - SPARE register bit
- *Bit14 DACSEL** - DAC programming enable common to all MTC/A DACs. Programming is initiated on the falling edge of this bit.
- *Bit15 DACCLK* - DAC programming clock common to all MTC/A DACs. One serial bit is clocked into DACs on the rising edge of this bit.

H.4 SOFT_GT Register

Writing to this register results in a 75ns raw trigger pulse being sent to global trigger logic (Section 8.1). This pulse will also act as the pulser when SP = 0 (See Sections 8.4 and H.2).

H.5 PWID Register

Pedestal width value between 0 and 254 which is latched on LOAD_ENPW. Pedestal width = $\overline{\text{PWID}} \times 5$ ns.

H.6 RTDEL Register

Coarse 10ns PED $\rightarrow$ PULSE_GT delay value between 0 and 254 which is latched on LOAD_ENPW. Coarse delay = $\overline{\text{RTDEL}} \times 10$ ns.

H.7 ADDEL Register

Fine <100ps PED $\rightarrow$ PULSE_GT delay value between 0 and 255. Fine delay $\approx$ ADDEL$\times$100 ps.

H.8 THRESHMON Register

Readback of trigger thresholds on MTC/As. Bits 0..11 are the digital ADC value for the selected threshold. The converted voltages are on the MTC/D, so calibration is required to determine the voltage difference between the MTC/D ADC and the MTC/A DACs. Bit 12 is a busy flag which indicates that a conversion was in process when the ADC output was latched.

H.9 PMSK Register

Pedestal fanout crate mask. Setting a given bit in this register corresponds to sending a particular crate any generated PED pulses. The first 20 bits are SNO crates while the last 5 are spares.

H.10 SCALE Register

SCALE value for the prescaling of NHIT_100_LO between 0 and 65534 which is latched on LOAD_ENPR. There will be one PRESCALE raw trigger for every $\overline{\text{SCALE}}$+1 NHIT_100_LO raw triggers.

H.11 BWR_ADD_OUT Register

Next memory write pointer. This is generated by the memory controller and denotes the next memory location which will be written to at the end of a normal trigger cycle.

H.12 BBA register

Memory read pointer. The lower 20 bits specify which memory location the controller will read from during the next memory read. The upper three bits specify which SIMM is read from in memory TESTMODE1.

H.13 GT_LOCK Register

Trigger LOCKOUT width value between 0 and 254 which is latched on LOAD_ENLK. The LOCKOUT width for synchronous GTRIGs is $\overline{\text{GTLOCK}} \times 20$ ns. For asynchronous triggers,

the LOCKOUT width will jitter up to $\approx$ 19ns less than the above value of the width for synchronous triggers.

H.14 MASK

Global trigger generation mask. Each bit in the register corresponds to allowing one raw trigger type to generate a global trigger as shown in Table 7.

Table 7: Global Trigger Mask

MASK Bit	Raw Trigger Masked In
0	NHIT_100_LO
1	NHIT_100_MED
2	NHIT_100_HI
3	NHIT_20
4	NHIT_20_LB
5	ESUM_LO
6	ESUM_HI
7	OWLN
8	OWLE_LO
9	OWLE_HI
10	PULSE_GT
11	PRESCALE
12	PEDESTAL
13	PONG
14	SYNC
15	EXT_ASYNC
16..21	EXT2..7
22	EXT8/PULSE_ASYNC
23	SPECIAL_RAW
24	NCD
25	SOFT_GT

H.15 XILINX_PROG Register

There are three XILINX FPGAs (Field Programmable Gate Arrays) on the MTC/D which contain logic specific to various functions of the board. The VME interface is contained in an XC3064A which is programmed automatically on power-up by an XC1765D serial PROM. The other two FPGAs are then programmed in a daisy-chain fashion through VME writes to this register and can be reprogrammed with new logic at any time. An XC3064A contains the FIFO memory controller and an XC3190A handles the numerous functions such as counter loading/clocking/latching, SYNCLR generation, error flag generation, and SPECIAL_RAW trigger logic. The following is the register structure:

- *Bit0 SDIN* - Serial data which contain the logic to be programmed as well as various header information. This line is sent to the memory controller FPGA which then transmits serial data to the other FPGA in a daisy-chain fashion.
- *Bit1 CCLK* - Configuration clock to inform the FPGAs when to latch the serial data bits. This line is common to both FPGAs.
- *Bit2 DNPR** - Input to DONE/PROGRAM* buffer (DONE/PROGRAM* will be explained later).
- *Bit3 PROG_EN* - Enable for DONE/PROGRAM* buffer. Controls whether or not to drive DNPR* level through the buffer to the FPGAs.
- *Bit4 PROGRAM** - Output of the DONE/PROGRAM* buffer which goes to both FPGAs. A high-to-low transition initiates a reprogramming of the FPGAs. At the completion of its programming, the FPGAs will attempt to drive this line high, which is the reason for the tri-state buffering of this signal.
- *Bit 5 PROGRAM** - This bit is read-only in that it is only driven by the PROGRAM* line discussed above. It is used to determine whether or not a successful programming of the FPGAs has occurred.

The programming sequence is briefly as follows: The DONE/PROGRAM* buffer is enabled with PROG_EN and a high-to-low transition is performed on DNPR* to initiate the

FPGA programming sequence. The serial data (SDIN) and configuration clock (CCLK) are then applied with the correct number of bits and clock cycles ($\approx 110,000$ for the MTC/D). Some time before the last configuration clock cycle, the DONE/PROGRAM* buffer is disabled with PROG_EN to allow the FPGAs to drive this line high indicating a successful configuation. The PROGRAM* line is then read back to verify programming. (For more detailed information on FPGAs and how to program them consult "The SNO 32-channel Front End Card" and Xilinx's "The Programmable Logic Data Book."

H.16 GMSK Register

Global trigger fanout crate mask. Setting a given bit in this register corresponds to sending a particular crate any generated GTRIG pulses. The first 20 bits are SNO crates while the last 5 are spares.

H.17 OCGT Register

Global trigger count. This read-only register outputs the GT count at the time the register is read.

H.18 C50_LOWER Register

50 MHz count (lower 32 bits). This read-only register outputs the 50 MHz count at the time the register is read.

H.19 C50_UPPER Register

50 MHz count (upper 11 bits). This read-only register outputs the 50 MHz count at the time the register is read.

H.20 C10_LOWER Register

10 MHz count (lower 32 bits). This read-only register outputs the 10 MHz count at the time the register is read.

H.21 C10_UPPER Register

10 MHz count (upper 21 bits). This read-only register outputs the 10 MHz count at the time the register is read.

I Getting the Schematics

A postscript version of the schematics for the trigger electronics can be obtained via anonymous ftp to

`ftp.hep.upenn.edu`

The files are in the directory

`/pub/neubauer/schematics`